Technical Reference

Tektronix

RT-Eye® PCI Express® Compliance Module Methods of Implementation (MOI)

071-2041-01

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1 Introduction to the RT-Eye PCI Express Compliance Module[1]

This document provides the procedures for making PCI Express compliance measurements with the Tektronix TDS6000 Series and TDS7704B, real time oscilloscopes (6 GHz models and above), the DPO/DSA70000 series and probing solutions.

The PCI Express (PCI-E) Compliance Module Version 2.0 (Opt. PCE) is an optional software plug-in to the RT-Eye Serial Data Compliance and Analysis software (Opt. RTE). The PCI Express Compliance module provides transmitter path measurements (amplitude, timing, and jitter), waveform mask testing, and Reference Clock (RefClk) compliance measurements described in multiple variants of the PCI Express specifications. Specifications covered in this document and the PCE module includes a total of eighteen data and reference clock test points defined in the following specifications.

Additional test points can also be added by the user, or provided by Tektronix representatives, using *Dynamic Test Point (DTP)* definition, described in detail in Section 9. Refer to the release notes (readme.txt) for information on the additional test point files that may have been added after this release.

Table 1 – Supported Specifications

Test Methods	Spec Revision	PCI Express Specification Title	Test Points Defined
Rev1.0a	Rev1.0a	Base Specification	Transmitter and Receiver (Section 4.3)
	Rev 1.0	Mobile Graphics Lower Power Addendum	Transmitter (Section 2.2)
	Rev1.0a	CEM (Card Electro-Mechanical) Specification	System and Add-In Card (Section 4.7)
	Rev 1.0a	PCMCIA Express Card Standard	Host System Transmitter Express Card Transmitter (Section 4.2.1.2)
Rev1.1	Rev1.1	Base Specification	Transmitter & Receiver (Section 4.3)
	Rev1.1	CEM Specification	System and Add-In Card (Section 4.7) Reference Clock (Section 2.1)
	Rev1.0	Express Module Specification	Transmitter Path and System Board (Section 5.4)
	Rev0.4C	External Cabling Specification	Transmitter and Receiver Path (Section 3.3)

[1] **Disclaimer:** The tests provided in the PCI Express compliance module (which are described in this document) do not guarantee PCI Express compliance. The test results should be considered "Pre-Compliance". Official PCI Express compliance and PCI-SIG Integrator List qualification is governed by the PCI-SIG (Special Interest Group) and can be achieved only through official PCI-SIG sanctioned testing.

Test Methods	Spec Revision	PCI Express Specification Title	Test Points Defined
	TBD	Future 2.5 Gb/s Variants	Dynamic Test Points as specifications are defined
Rev2.0	Rev2.0	Base Specification	Transmitter & Receiver (Section 4.4) Mobile Low Power Transmitter (Section 4.4)
	Rev2.0	CEM Specification	System and Add-In Card (Section 4.7)
	TBD	Future 5 Gb/s Variants	Dynamic Test Points as specifications are defined

Refer to http://www.pcisig.com/specifications/pciexpress/ for the latest specifications.

The PCE module can also be used to automate setup procedures for SigTest by using its *SigTest Import* feature (Refer to Section 8).

In this document, for all references to the PCI Express Base Specification and Card Electrical Mechanical (CEM) specification, refer to all versions of the Spec. (Rev 1.0a, 1.1, and 2.0). Differences between the specifications are specifically called out when appropriate.

In the subsequent sections, step-by-step procedures are described to help you perform PCI Express measurements. Each measurement is described as a Method of Implementation (MOI). For further reference, consult the Compliance checklists offered to PCI-SIG members at www.pcisig.com.

2 PCI Express Compliance Specifications

As shown in Table 1, Electrical Specifications for PCI Express are provided in multiple documents. This section provides a summary of the measurement parameters measured in the RT-Eye PCE module and how they are related to the symbol and test limits in the specification.

2.1 Differential Transmitter (TX) Output Specifications

The following table shows the available measurements in the PCE Module and their test limits defined in each of the Base specifications.

Table 2- Supported base specification transmitter measurements

Parameter	Symbol(s)	Specification		
		2.5 GT/s Rev1.0a	2.5 GT/s Rev1.1	5.0 GT/s Rev2.0
Unit interval	*UI*	400 ps +/- 300 ppm	400 ps +/- 300 ppm	200 ps +/- 300 ppm
Differential p-p TX voltage swing	$V_{TX-DIFFp-p}$ $V_{TX-SWING}$	0.8 V (min) 1.2 V (max)	0.8 V (min) 1.2 V (max)	0.8 V (min) 1.2 V (max)
Low power differential p-p TX voltage swing	$V_{TX-SWING-LOW}$	Not Specified	Not Specified	0.4 V (min) 0.7 V (max)
De-emphasized output voltage ratio	$V_{TX-DE-RATIO}$	-3.0 dB (min) -4.0 dB (max)	-3.0 dB (min) -4.0 dB (max)	-5.5 dB (min) -6.5 dB (max) or -3.0 dB (min) -4.0 dB (max)
Instantaneous lane pulse width [2]	$T_{MIN-PULSE}$	Not Specified	Not Specified	0.9 UI (min)
Transmitter eye including all jitter sources	T_{TX-EYE} t_{TX-EYE_TJ}	0.70 UI (min)	0.75 UI (min)	0.75 UI (min)
Maximum time between the jitter median and maximum deviation from the median	$T_{TX-EYEMEDIAN-to-MAXJITTER}$	0.125 UI (max)	.125 UI (max)	Not Specified
Deterministic jitter	$T_{TX-DJ-DD}$			0.15 UI (max)
D+/D- TX output rise/fall Time [3]	$T_{TX-RISE}$ $T_{TX-FALL}$	0.125 UI (min)	0.125 UI (min)	0.15 UI (min)
AC RMS common mode output voltage	$V_{TX-CM-ACp}$	20 mV (max)	Not Specified	Not Specified
Absolute delta of DC common mode voltage between D+ and D-	$V_{TX-CM-DC-LINE-DELTA}$	0 V (min) 25 mV (max)	0 V (min) 25 mV (max)	0 V (min) 25 mV (max)

[2] Instantaneous lane pulse width defined in the Gen2 specification is not supported in the RT-Eye PCI Express Compliance module. It is recommended that TDSJIT3 Advanced Jitter Analysis Data Period (Min) be used for this measurement.

[3] Rise/Fall time measurements in RT-Eye PCI Express Module are compliant to the Rev1.0a and Rev1.1 specification. For Gen2, rise and fall time is limited to TF2 and TR2 as defined in section 4.3.3.8 of the Base Specification

2.2 Differential Transmitter (TX) Compliance Eye Diagrams

Figure 1a shows the eye mask definitions for the Rev1.1 Base specification. It provides an example of a transmitter mask for a signal with de-emphasis. Transition and non-transition bits must be separated to perform the mask testing. The amplitude and jitter mask geometries are derived from the amplitude and jitter specifications. Low power transmitter variants in both Gen1 and Gen2 do not use de-emphasis (This is shown in Figure 1b).

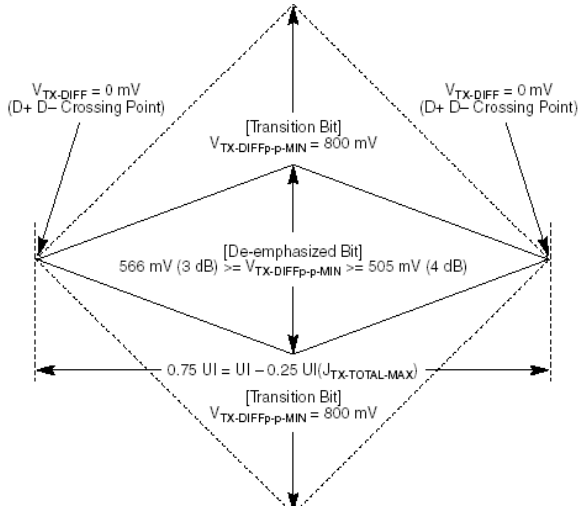


Figure 1a: Transmitter eye masks for transition and non-transition bits

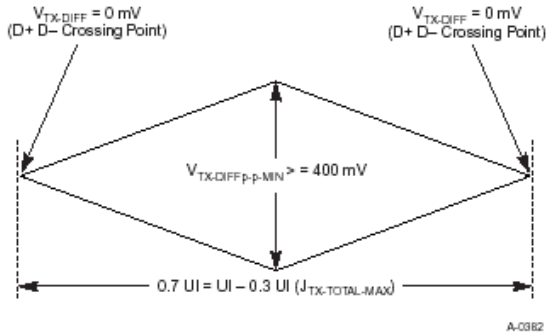


Figure 1b: Transmitter eye mask for low power variant where de-emphasis is not used

2.3 Differential Receiver (RX) Input Specifications

The following table shows the available measurements in the PCE Module and their test limits defined in each of the Base specifications.

Table 3 – Supported base specification receiver measurements

Parameter	Symbol	2.5 GT/s Rev1.0a	2.5 GT/s Rev1.1	5.0 GT/s Rev2.0
Unit interval	*UI*	400 ps +/- 300 ppm	400 ps +/- 300 ppm	200 ps +/- 300 ppm
Minimum receiver eye height	V_{RX_EYE}	0.175 V (min) 1.2 V (max)	0.175 V (min) 1.2 V (max)	0.120 V (min) 1.2 V (max)
Minimum receiver eye width	T_{RX-EYE}	0.40 UI (min)	0.40 UI (min)	0.40 UI (min)
Receiver deterministic jitter –Dj	$T_{RX\_DJ\_DD}$	Not Specified	Not Specified	0.44 UI (max)
Maximum time between the jitter median and maximum deviation from the median.	$T_{TX\text{-}EYEMEDIAN\text{-}to\text{-}MAXJITTER}$	0.30 UI (max)	0.30 UI (max)	Not Specified

2.4 Differential Receiver (RX) Compliance Eye Diagrams

Figure 2 shows the receiver eye mask definitions for the Rev1.1 Base specification. The amplitude and jitter mask geometries are derived from the amplitude and jitter specifications.

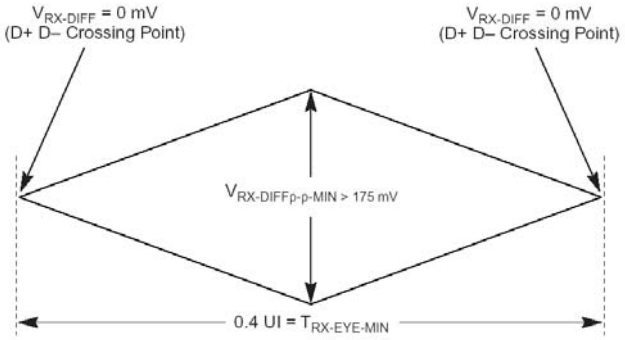


Figure 2: Receiver input eye mask

2.5 Add-In Card Transmitter Path Compliance Specifications

Table 4 is derived from the Electrical Mechanical Specifications (CEM). See the CEM Specification for additional notes and test definitions.

Table 4 – Supported CEM add-in card measurements

Parameter	Symbol	2.5 GT/s Rev1.0a	2.5 GT/s Rev1.1	5.0 GT/s Rev2.0	5.0 GT/s Rev2.0
DeEmphasis Setting		3.5 dB	3.5 dB	3.5 dB	6.0 dB
Unit interval	*UI*	400 ps +/- 300 ppm	400 ps +/- 300 ppm	200 ps +/- 300 ppm	200 ps +/- 300 ppm
Eye height of transition bits	V_{TXA}	0.514 V (min) 1.2 V (max)	0.514 V (min) 1.2 V (max)	0.380 V (min) 1.2 V (max)	0.306 V (min) 1.2 V (max)
Eye height of non-transition bits	V_{TXA_d}	0.360 V (min)	0.360 V (min)	0.380 V (min)	0.260 V (min)
Eye width across any 250 UIs	T_{TXA} *In Rev1.0a*	237 ps (min)	Not Specified	Not Specified	Not Specified
Eye width with sample size of 10^6 UI	T_{TXA} *In Rev1.1*	Not Specified	287 ps (min)	Not Specified	Not Specified
Jitter eye opening at BER 10^{-12}	T_{TXA} *In Rev2.0*	Not Specified	274 ps (min)	123 ps (min) with Crosstalk	123 ps (min) with Crosstalk
Total Jitter at BER 10^{-12}	*Tj at BER* 10^{-12}	Not Specified	Not Specified	77 ps (max)	77 ps (max)
Deterministic Jitter at BER 10^{-12}	*Max Dj*	Not Specified	Not Specified	57 ps (max)	57 ps (max)
Maximum median-max jitter outlier with sample size of 10^6 UI	$J_{TXA\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	Not Specified	56.5 ps (max)	Not Specified	Not Specified
Maximum median-max jitter outlier with sample size of 10^6 UI		Not Specified	63 ps (max)	Not Specified	Not Specified

2.6 Add-In Card Compliance Eye Diagrams

The amplitude and jitter masks are derived from the amplitude and jitter specifications in Table 4.

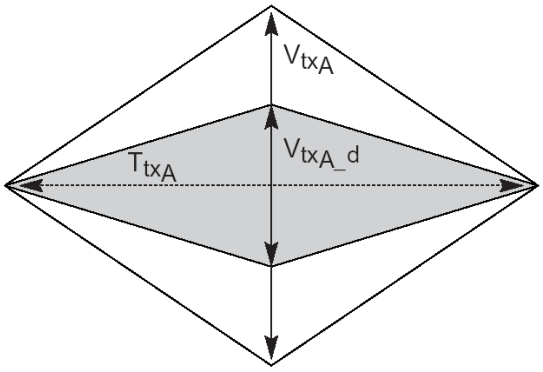


Figure 3: Add-in card compliance eye masks

2.7 System Board Transmitter Path Compliance Eye Diagrams

Table 5 is derived from the Electrical Mechanical Specifications (CEM). See the CEM Specification for additional notes and test definitions.

Table 5 – Supported CEM System Board Measurements

Parameter	Symbol	2.5 GT/s Rev1.0a	2.5 GT/s Rev1.1	5.0 GT/s4 Rev2.0
Unit interval	*UI*	400 ps +/- 300 ppm	400 ps +/- 300 ppm	200 ps +/- 300 ppm
Eye height of transition bits	V_{TXS}	0.274 V (min) 1.2 V (max)	0.274 V (min) 1.2 V (max)	0.300 V (min) 1.2 V (max)
Eye height of non-transition bits	V_{TXS_d}	0.253 V (min)	0.253 V (min)	0.300 V (min)
Eye width across any 250 UIs	T_{TXS} *In Rev1.0a*	183 ps (min)	Not Specified	Not Specified
Eye width with sample size of 10^6 UI	T_{TXS} *In Rev1.1*	Not Specified	246 ps (min)	Not Specified
Jitter eye opening at BER 10^{-12}	T_{TXS} *In Rev2.0*	Not Specified	233 ps (min)	95 ps (min) with Crosstalk
Maximum median-max jitter outlier with sample size of 10^6 UI	$J_{TXA\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	Not Specified	77 ps (max)	Not Specified
Maximum median-max jitter outlier with sample size of 10^6 UI		Not Specified	83.5 ps (max)	TBD

2.8 System Board Compliance Eye Diagrams

The amplitude and jitter masks are derived from the amplitude and jitter specifications in Table 5.

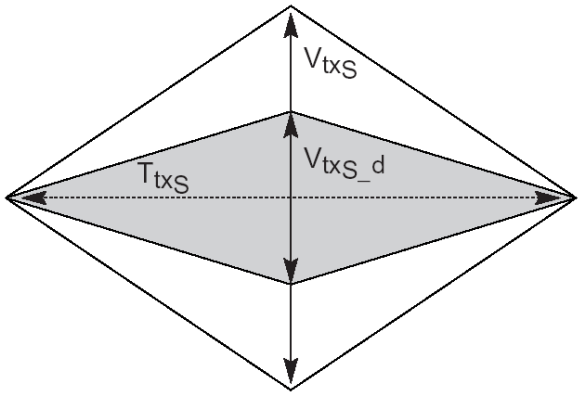


Figure 4: System Board Compliance Eye Masks

[4] At 5GT/s, the PCI Express 2.0 CEM specification requires dual port measurement. The dual port measurement requires differential Clock and Data capture and analysis, which is not supported in the RT-Eye. The test point offered in the RT-Eye software recovers the clock from the data signal. For dual port measurements, PCI-SIG SigTest version 3.0 and above is recommended.

2.9 PCI ExpressModule™ Compliance Specifications

The specifications in this section are taken from the PCI Express ExpressModule™ specification, which is a companion specification to the *PCI Express Base specification*. Its primary focus is the implementation of a modular I/O form factor that is focused on the needs of workstations and servers. Measurements in the PCE module support add-in card and system transmitter path measurements at the PCI Express connector.

2.9.1 ExpressModule Add-In Card Transmitter Path Specifications

Table 6 is derived from Section 5.4.1 of the ExpressModule Electro-Mechanical Specifications Rev1.0.

Table 6 – Supported ExpressModule Add-In Card Measurements

Parameter	Symbol	Rev1.0
Unit interval	*UI*	400 ps +/- 300 ppm
Eye height of transition Bits	V_{TXA}	0.514 V (min) 1.2 V (max)
Eye height of non-transition Bits	V_{TXA_d}	0.360 V (min)
Eye width with sample size of 10^6 UI	T_{TXA} In Rev1.1	287 ps (min)
Jitter eye opening at BER 10^{-12}		274 ps (min)
Maximum median-max jitter outlier with sample size of 10^6 UI	$J_{TXA\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	56.5 ps (max)
Maximum median-max jitter outlier with sample size of 10^6 UI		63 ps (max)

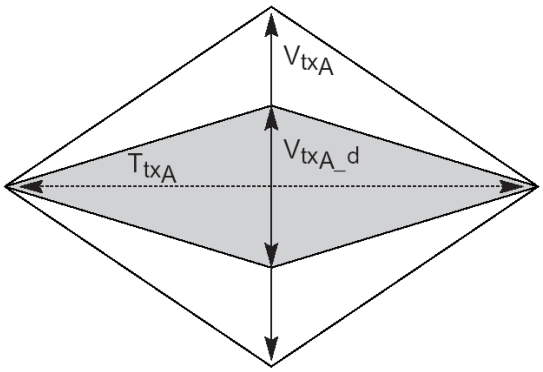


Figure 5: ExpressModule add-in card compliance eye masks

2.9.2 ExpressModule System Board Transmitter Path Compliance Eye Diagrams

Table 7 is derived from Section 5.4.3 of the ExpressModule Electro-Mechanical Specifications Rev1.0.

Table 7 – Supported ExpressModule system board measurements

Parameter	Symbol	Gen1 Rev1.0
Unit interval	*UI*	400 ps +/- 300 ppm
Eye height of transition bits	V_{TXS}	0.274 V (min) 1.2 V (max)
Eye height of non-transition bits	V_{TXS_d}	0.253 V (min)
Eye width with sample size of 10^6 UI	T_{TXS}	246 ps (min)
Jitter eye opening at BER 10^{-12}		233 ps (min)
Maximum median-max jitter outlier with sample size of 10^6 UI	$J_{TXA\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	77 ps (max)
Maximum median-max jitter outlier with sample size of 10^6 UI		83.5 ps (max)

2.9.3 Express Module System Board Compliance Eye Diagrams

The amplitude and jitter masks are derived from the amplitude and jitter specifications in Table 7.

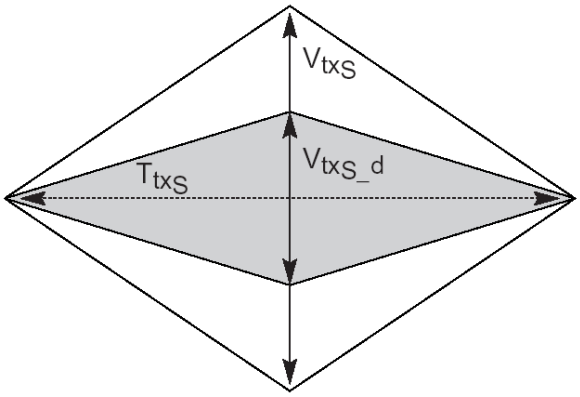


Figure 6: ExpressModule system board compliance eye masks

2.10 PCI Express External Cabling Specifications

The specifications in this section are taken from the PCI Express External Cabling Specification. Its primary focus is the implementation of a cabled interconnect. Measurements in the PCE module support transmitter path and receiver path measurements. These measurements represent the test points at the transmitter end of the cable and the receiver end of the cable respectively.

2.10.1 External Cabling Transmitter Path Specifications

Table 8 is derived from Section 3.3.1 of the External Cabling Specification Rev. 0.4C.

Table 8 – Supported external cabling transmitter path measurements

Parameter	Symbol	Rev0.4C
Unit interval	*UI*	400 ps +/- 300 ppm
Eye height of transition bits	V_{TXA}	0.659 V (min) 1.2 V (max)
Eye height of non-transition bits	V_{TXA_d}	0.456 V (min)
Eye width with sample size of 10^6 UI	T_{TXA}	309 ps (min)
Jitter eye opening at BER 10^{-12}		296 ps (min)

2.10.2 Cable (Transmitter Side) Eye Diagrams

The amplitude and jitter masks are derived from the amplitude and jitter specifications in Table 8.

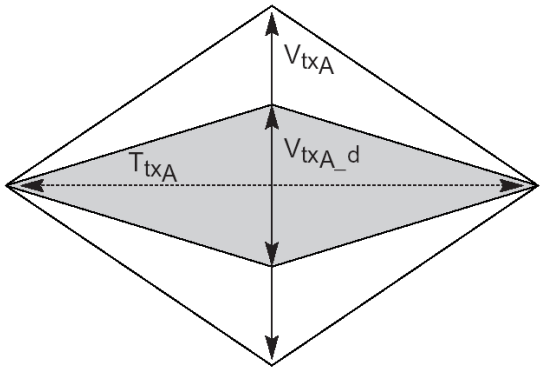


Figure 7: Cable (transmitter side) compliance eye masks

2.10.3 External Cabling Receiver Path Specifications

Table 9 is derived from Section 3.3.2 of the External Cabling Specification Rev. 0.4C.

Table 9 – Supported CEM system board measurements

Parameter	Symbol	Gen1 Rev1.0
Unit interval	*UI*	400 ps +/- 300 ppm
Eye height of transition bits	V_{RXA}	0.219 V (min) 1.2 V (max)
Eye height of non-transition bits	V_{RXA_d}	0.200 V (min)
Eye width with sample size of 10^6 UI	T_{RXA}	247 ps (min)
Jitter eye opening at BER 10^{-12}		234 ps (min)

2.10.4 Cable (Receive Side) Eye Diagrams

The amplitude and jitter masks are derived from the amplitude and jitter specifications in Table 9.

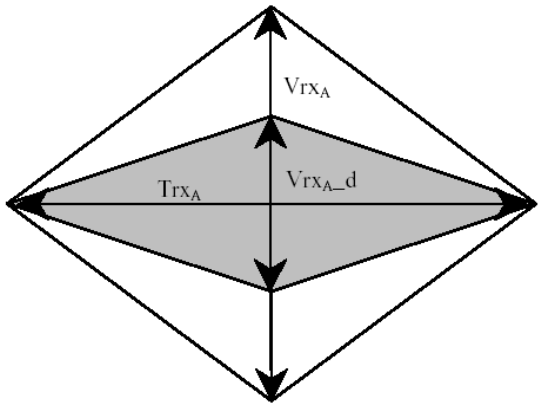


Figure 8: Cable (receiver side) compliance eye masks

2.11 PCMCIA ExpressCard™ Specifications

The specifications in this section are taken from the PCMCIA ExpressCard Standard (Release 1.0). Its primary focus is a small modular add-in card technology based on PCI Express and USB interfaces. Measurements in the PCE module support host system and ExpressCard transmitter path measurements.

2.11.1 ExpressCard - Module Transmitter Path Specifications

Table 10 is derived from Section 4.2.1.3.2 of the ExpressCard Specification Release 1.0.

Table 10 – Supported ExpressCard transmitter path measurements

Parameter	Symbol	Release 1.0
Unit interval	*UI*	400 ps +/- 300 ppm
Eye height of transition bits	V_{TXA}	538 V (min) 1.2 V (max)
Eye height of non-transition bits	V_{TXA_d}	0.368 V (min)
Eye width across any 250 UIs	T_{TXA}	237 ps (min)

2.11.2 ExpressCard Transmitter Path Eye Diagrams

The amplitude and jitter masks are derived from the amplitude and jitter specifications in Table 10.

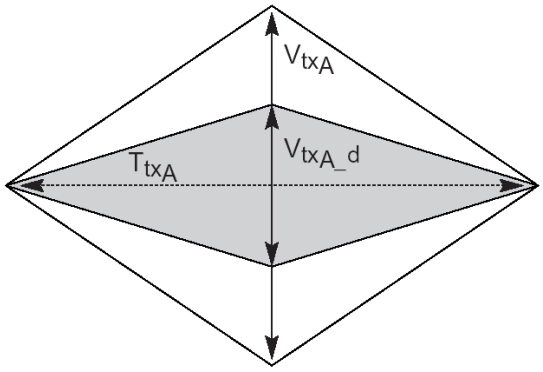


Figure 9: ExpressCard Module Transmitter compliance eye masks

2.11.3 ExpressCard - Host System Transmitter Path Specifications

Table 11 from Section 4.2.1.3.2 of the ExpressCard Specification Release 1.0.

Table 11 – Supported ExpressCard Host System Transmitter Path Measurements

Parameter	Symbol	Release 1.0
Unit interval	*UI*	400 ps +/- 300 ppm
Eye height of transition bits	V_{txS}	0.262 V (min) 1.2 V (max)
Eye height of non-transition bits	V_{txS_d}	0.247 V (min)
Eye width across any 250 UIs	T_{TxS}	183 ps (min)

2.11.4 ExpressCard – Host System Eye Diagrams

The amplitude and jitter masks are derived from the amplitude and jitter specifications in Table 11.

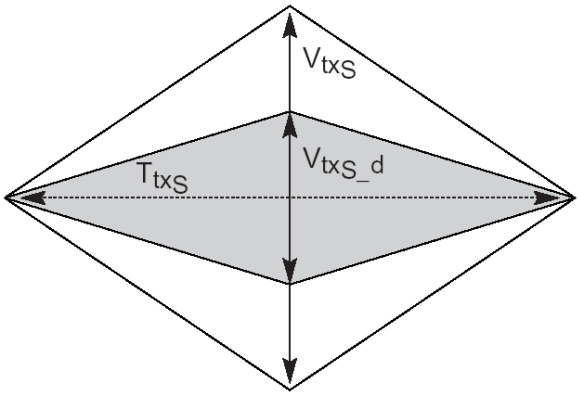


Figure 10: ExpressCard Host System compliance eye masks

2.12 Reference Clock Compliance Specifications

Table 12 is derived from Section 2.1 of the Gen1 Rev1.1 Electrical Mechanical Specifications (CEM). Reference Clock measurements for Rev2.0 are not currently supported in RT-Eye.

Table 12 – Supported reference clock measurements

Parameter	Symbol	Gen1 Rev1.1	5.0 GT/s Rev2.0
Rise edge rate	*Rise Edge Rate*	0.6 V/ns (min) 4.0 V/ns (max)	Not supported In RT-Eye software. For Rev2.0 RefClk Compliance tools, refer to the tools library at www.pcisig.com
Fall edge rate	*Fall Edge Rate*	0.6 V/ns (min) 4.0 V/ns (max)	
Differential input high voltage	V_{IH}	150 mV (max)	
Differential input low voltage	V_{IL}	-150 mV (min)	
Absolute period (including jitter and spread spectrum)	T_{PERIOD_ABS}	9.847 ns (min) 10.203 ns (max)	
Duty cycle	*Duty Cycle*	40% (min) 60% (max)	
Maximum peak-peak filtered phase jitter	*Jitter @ 10^{-12} BER*	108 ps (max)	
Maximum peak-peak filtered phase jitter	*Jitter @ 10^{-6} BER*	86 ps (max)	
RMS jitter	T_{CLK_RJ}		

3 Preparing to Take Measurements

3.1 Required Equipment

The following equipment is required to take the measurements:

- Oscilloscope Selection:
  - Gen1 (2.5 Gb/s) – The PCI-SIG recommends a minimum of 6 GHz system BW for Gen1 Measurements. Tektronix models that meet this recommendation include: All the TDS6000B/C series instruments, TDS7704B, and the DPO/DSA70000 series.
  - Gen2 (5 Gb/s) – It is recommended that >12 GHz system BW is used for Gen2. This ensures that the 5th harmonic is represented in the measurements. Tektronix models that meet this recommendation are TDS6000C models.
- RT-Eye software (Opt. RTE) and PCI Express Compliance Module (PCE) installed.
- Probes – Probing configuration is MOI specific. Refer to each MOI for proper probe configuration.
- Test fixture breakout from transmitter to differential SMA connectors. The Compliance Base Board (CBB) used for add-in card compliance tests and a Compliance Load Board (CLB) used for system compliance tests are available through the PCI-SIG at the following URL: http://www.pcisig.com/specifications/ordering_information/ordering_information
- Test fixtures for ExpressCard testing are available from the following URL: http://www.expresscard.org/web/site/testtools.jsp

3.2 Probing Options for Transmitter Testing

The first step is to probe the link. Use one of the following four methods to connect probes to the link.

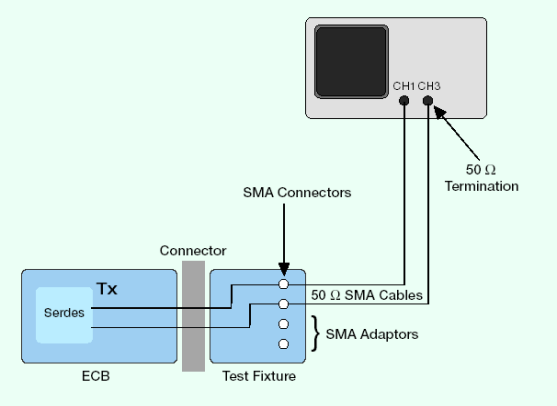
Table 13 – Example Probing configurations for a PCI express link

		Probing Configurations			Captured Waveforms		Typical System Specifications									
							TDS6604/B		TDS7704B**		TDS6804B		TDS6124C		TDS6154C	
		Probe	Break Serial Link	Channels Used	Differential Mode	Common Mode	Band Width	Rise* Time (20-80)	Band Width	Rise* Time (20-80)	Band Width	Rise* Time (20-80)	Band Width	Rise* Time (20-80)	Band Width	Rise* Time (20-80)
SMA Connection	A	2 x TCA-SMA	Y	2	Pseudo	AC	6GHz	53ps	7GHz	43ps	8GHz	35ps	12GHz	24ps	15GHz	19ps
	B	1 x P7380SMA	Y	1	True	No	6GHz	53ps	7GHz	43ps	8GHz	35ps	8GHz	35ps	8GHz	35ps
ECB Pad Connection	C	2 x P7260	Y or N	2	Pseudo	AC/DC	6GHz	53ps	6GHz	56ps	6GHz	56ps	6GHz	56ps	6GHz	56ps
		2 x P7380	Y or N	2	Pseudo	AC/DC	6GHz	53ps	7GHz	43ps	8GHz	35ps	8GHz	35ps	8GHz	35ps
		2 x P7313	Y or N	2	Pseudo	AC/DC	6GHz	53ps	7GHz	43ps	8GHz	35ps	12GHz	28ps	12.5GHz	25ps
	D	1 x P7380	Y or N	1	True	No	6GHz	53ps	7GHz	43ps	8GHz	35ps	8GHz	35ps	8GHz	35ps
		1 x P7313	Y or N	1	True	No	6GHz	53ps	7GHz	43ps	8GHz	35ps	12GHz	28ps	12.5GHz	25ps

** Typical*
*** 10GS/s in Pseudo-differential*

3.2.1 SMA Input Connection

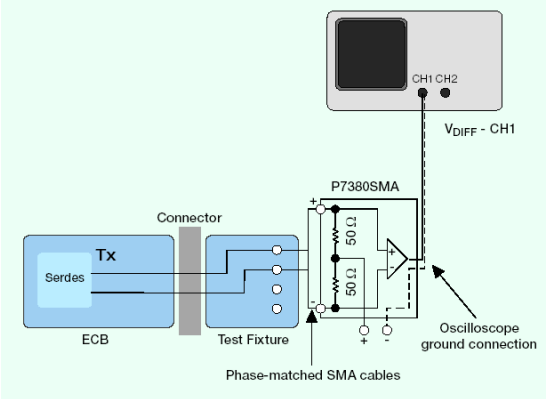
1. **Two TCA-SMA inputs using SMA cables (Ch1) and (Ch3)**
   The differential signal is created by the RT-Eye software from the math waveform Ch1-Ch3. The Common mode AC measurement is also available in this configuration from the common mode waveform (Ch1+Ch3)/2. This probing technique requires breaking the link and terminating into a 50 Ω/side termination of the oscilloscope. While in this mode, the PCI Express SerDes will transmit the compliance test pattern. Ch-Ch de-skew is required using this technique because two channels are used. This configuration does not compensate for cable loss in the SMA cables. The measurement reference plane is at the input of the TCA-SMA connectors on the oscilloscope. Any cable loss should be measured and entered into the vertical attenuation menu for accurate measurements at the SMA cable attachment point.



Probe Configuration A

SMA Psuedo-differential

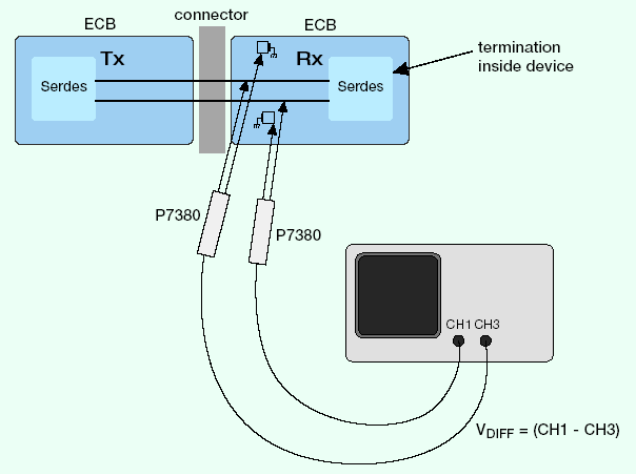
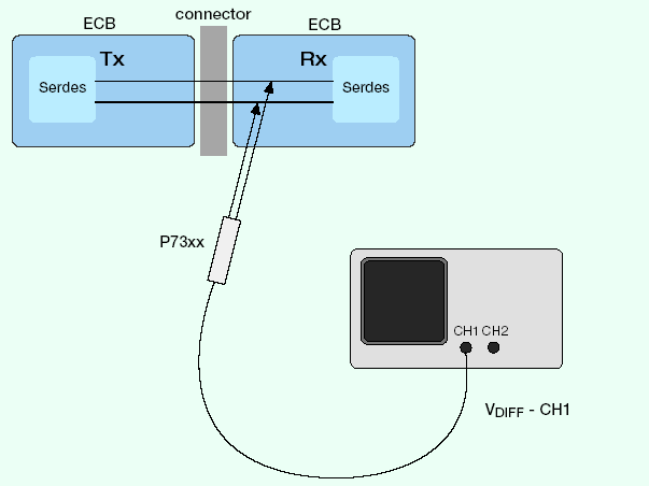
2. **One P7300SMA series differential active probe (Ch1)**
   The differential signal is measured across the termination resistors inside the P7300SMA series probe. This probing technique requires breaking the link. While in this mode, the PCI Express SerDes will transmit the compliance test pattern. Matched cables are provided with the probe to avoid introducing de-skew into the system. Only one channel of the oscilloscope is used. The P7300SMA provides a calibrated system at the Test Fixture attachment point, eliminating the need to compensate for cable loss associated with the probe configuration A.



Probe Configuration B

SMA Input Differential Probe

3.2.2 ECB Pad Connection

3. **Two active probes (Ch1) and (Ch3)** The differential signal is created by the RT-Eye software from the math waveform Ch1-Ch3. The Common mode AC measurement is also available in this configuration from the common mode waveform (Ch1+Ch3)/2. This probing technique can be used for either a live link that is transmitting data, or a link that has terminated into a "dummy load". In both cases, the single-ended signals should be probed as close as possible to the termination resistors on both sides with the shortest ground connection possible. Ch-Ch de-skew is required using this technique because two channels are used.	 Probe Configuration C Two Single-Ended Active Probes
4. **One P7300 series Differential probe (Ch1)** The differential signal is measured directly across the termination resistors. This probing technique can be used for either a live link that is transmitting data, or a link that is terminated into a "dummy load". In both cases, the signals should be probed as close as possible to the termination resistors. De-skew is not necessary because a single channel of the oscilloscope is used.	 Probe Configuration D One Differential Active Probe

3.3 Initial Oscilloscope Setup

After connecting the DUT by following the proper probing configuration for the test, click **DEFAULT SETUP** and then **Autoset** to display the serial data bit stream.

3.4 Running the RT-Eye Software

1. On non-B or non-C model oscilloscopes (Example: TDS6604), Go to **File** > **Run Application** > **RT-Eye Serial Compliance and Analysis**. For B and C models (Example: TDS7704B, TDS6154C), go to **App** > **RT-Eye Serial Compliance and Analysis**. On DPO/DSA7000 series, go to **Analysis > RT- Eye Serial Compliance and Analysis.**

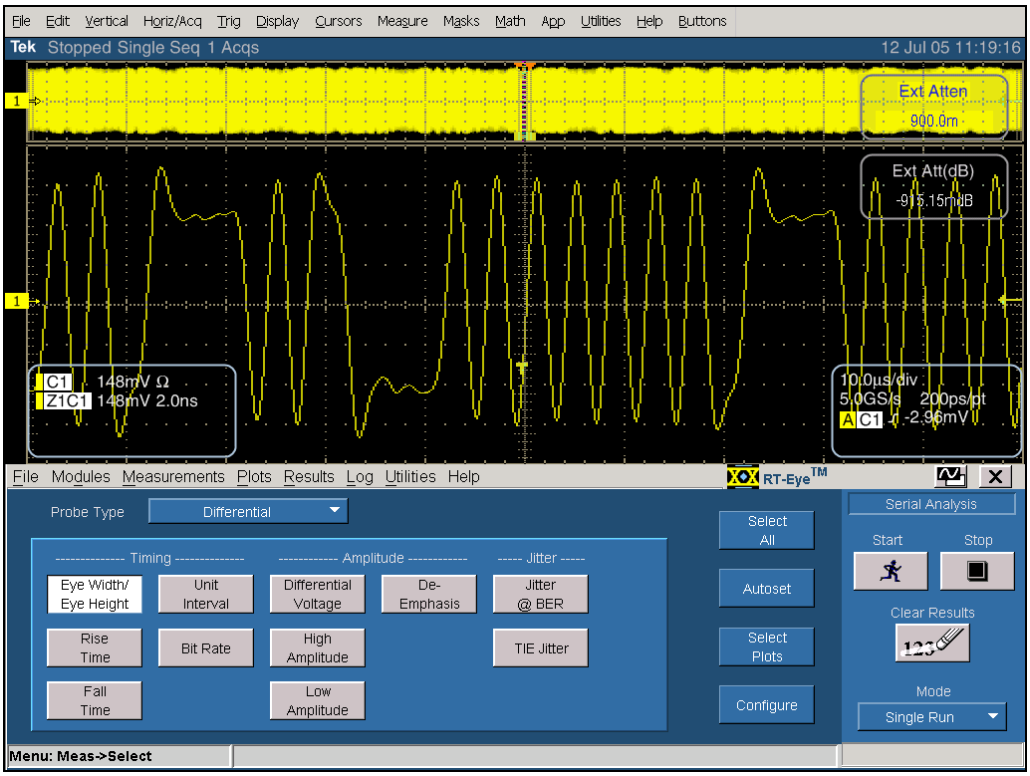


Figure 11: Default menu of the RT-Eye software

Figure 11 shows the oscilloscope display. The default mode of the software is the Serial Analysis module (Opt.RTE). This software is intended for generalized Serial Data analysis on copper serial data links.

2. Select the PCI Express Compliance Module from the **Modules** drop-down list.

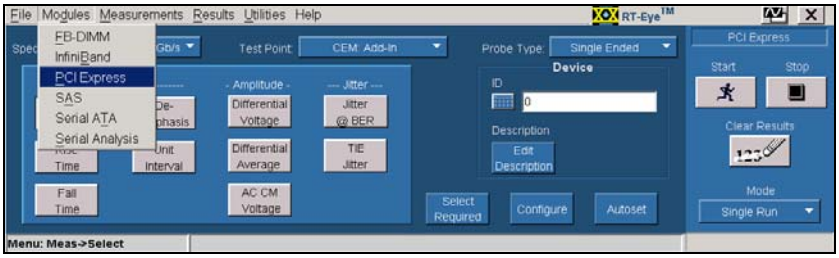


Figure 12: Choosing PCI Express Compliance Module.

Note: If PCI Express does not appear in the list (as in Figure 12), the PCI Express Compliance Module (Opt. PCE) has not been installed.

The rest of this MOI document details the use of the PCI Express Compliance Module to perform electrical compliance measurements.

For additional information, refer to the online help for the RT-Eye software available through the Serial Analysis Module help menu.

3.5 Configuring the Software to take measurements

Before you take compliance measurements, configure the software as follows:

3.5.1 Select Standard

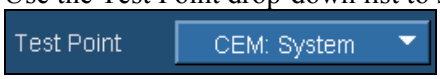
Using the Specification drop-down menu, select the desired specification to be measured.

The selections are:

- Rev1.0a – 2.5 Gb/s
- Rev1.1 – 2.5 Gb/s
- Gen2 – 5 Gb/s
- Use SIG-TEST – refer to Section 8

3.5.2 Select Test Point

Use the Test Point drop-down list to select the desired test point.



Selections in the Test Point menu are dependent on the selected specification. The selections are as follows:

If **Rev1.0a – 2.5 Gb/s** is selected as **Standard:**

- Receiver
- Driver
- CEM: Add-In
- CEM: System
- ExpressCard Module Tx
- ExpressCard Host Tx
- Mobile LP: Transmitter
- User Defined – Using Dynamic Test Points – See Section 9 for definition

If **Rev1.1 – 2.5 Gb/s** is selected as **Standard:**

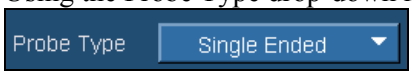
- Base: Transmitter
- Base: Receiver
- CEM: Add-In
- CEM: System
- Cable: Transmitter
- Cable: Receiver
- ExpressModule: System TX
- ExpressModule: TX Path
- User Defined – Using Dynamic Test Points – See Section 9 for definition
- Reference Clock

If **Gen2 – 5Gb/s** is selected as **Standard:**

- Base - Tx -6dB DeEmph
- Base - Tx -3.5dB DeEmph
- Base: Receiver
- User Defined – Using Dynamic Test Points – See Section 9 for definition
- Reference Clock

3.5.3 Select Probe Type

Using the Probe Type drop-down menu, select the desired probing configuration.



The selections are:

- Single-Ended – Select if Pseudo-differential (probing configurations A or C from Section 3.2) is being used.
- Differential – Select if true differential (probing configurations B or D from Section 3.2) is being used.

3.5.4 Select Measurements

In the **Measurement > Select** menu, select the desired measurements. Measurements can be selected either manually or as a group by using **Select Required**. If a measurement has a pass/fail limit associated with it in the test point file, it will be selected when **Select Required** is clicked. Measurements with pass/fail limits will show up in the **Results Summary** panel when the compliance test is run. Measurement results of selected measurements, which do not have limits associated with them can be viewed in the **Results Details** panel.

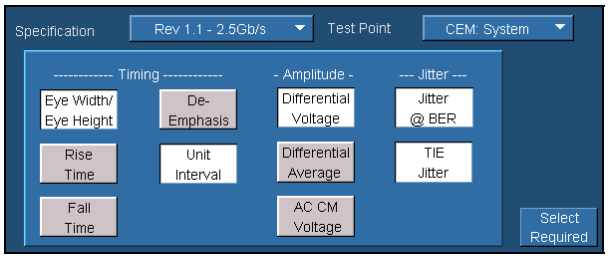


Figure 13: Measurement Select menu

For Compliance measurements, the following table indicates the PCI Express parameter (listed by symbol in the specification), the measurement to select in the Measurement Select Menu, and the results that appear in the Results Summary panel after the compliance test is complete. Refer to the tables in Section 2 for Pass/Fail limit criteria by specification.

Table 14 – Measurement Select/Result Cross Reference (Transmitter Test Points)

Parameter to measure	Symbol(s)	Selection in Measurement > Select Menu	Results in Measurement Results Summary
Unit interval	*UI*	Unit Interval	Unit Interval (Min) Unit Interval (Max)
Differential p-p TX voltage swing	$V_{TX-DIFFp-p}$ $V_{TX-SWING}$	Differential Voltage	Differential Voltage (Min) Differential Voltage (Max)
Low power differential p-p TX voltage swing	$V_{TX-SWING-LOW}$	Differential Voltage	Differential Voltage (Min) Differential Voltage (Max)
De-emphasized output voltage ratio	$V_{TX-DE-RATIO}$	De-Emphasis	De-Emphasis (Min) De-Emphasis (Max)
Instantaneous lane pulse width [5]	$T_{MIN-PULSE}$	Not supported in RT-Eye PCI-E Compliance Module use TDSJIT3 Data Period measurement	Data Period (Min)
Transmitter eye including all jitter sources	T_{TX-EYE} t_{TX-EYE_TJ}	For Gen1: Eye Width For Gen2: Jitter@BER	Gen1: Eye Width (Min) Gen2: Jitter Eye Opening (Min)
Maximum time between the jitter median and maximum deviation from the median	$T_{TX-EYEMEDIAN-to-MAXJITTER}$	For Gen1: TIE Jitter For Gen2: Not Specified	Gen1: TIE Jitter (Min) or TIE Jitter (Max); whichever value has the maximum deviation from the Median.

[5] Instantaneous lane pulse width defined in the Gen2 specification is not supported in the RT-Eye PCI Express Compliance module. It is recommended TDSJIT3 Advanced Jitter Analysis Data Period (Min) be used for this measurement.

Deterministic jitter	$T_{TX\text{-}DJ\text{-}DD}$	For Gen1: Not Specified For Gen2: Jitter@BER	Gen1: Not Specified Gen2: Deterministic Jitter (Max)
D+/D- TX output rise/fall Time[6]	$T_{TX-RISE}$ $T_{TX-FALL}$	Rise Time Fall Time	Rise Time (Min) Fall Time (Min)
AC RMS common mode output voltage	$V_{TX-CM-ACp}$	Gen1: AC CM Voltage Gen2: Not Specified	AC CM Voltage (Max)
Absolute delta of DC common mode voltage between D+ and D-	$V_{TX-CM-DC-LINE-DELTA}$	Differential Average	DifferentialAverageVoltage(Max)

Table 15 – Measurement Select/Result Cross Reference (Eye Diagram Testing for all test points)

Parameter	Symbol	Selection in Measurement > Select Menu	Results in Measurement Results Summary
Unit interval	*UI*	Unit Interval	Unit Interval (Min) Unit Interval (Max)
Eye height of transition bits	V_{TXA}	Eye Height	EyeH: TransBits (Min) EyeH: TransBits (Max)
Eye height of non-transition bits	V_{TXA_d}	Eye Height	EyeH: NonTrBits (Min) EyeH: NonTrBits (Max)
Receiver or all bits eye height	V_{RX_EYE}	Eye Height	EyeH: All Bits (Min) EyeH: All Bits (Max)
Eye width across any 250 UIs	T_{TXA} *In Rev1.0a*	Rev1.0a Only: Eye Width (for each 250 bit window)	Eye Width (Min)
Eye width with sample size of 10^6 UI	T_{TXA} *In Rev1.1*	Rev1.1 Only; Eye Width (sampled over 10^6 UIs)	Eye Width (Min)
Jitter eye opening at BER 10^{-12}	T_{TXA} *In Rev2.0*	Rev1.1 and Rev2.0 Jitter@BER	Jitter Eye Opening (Min)
Maximum median-max jitter outlier with sample size of 10^6 UI	$J_{TXA\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	Rev1.1 Only: TIE Jitter (sampled over 10^6 UIs)	TIE Jitter (Min) or TIE Jitter (Max); whichever value has the maximum deviation from the Median.

[6] Rise/Fall time measurements in RT-Eye PCI Express Module are compliant to the Rev1.0a and Rev1.1 specification. For Rev2.0, rise and fall time is limited to TF2 and TR2 as defined in the Base Specification.

3.5.5 Configure Source of Waveforms

Use the **Measurements > Configure > Source** menu to select the source of the measured data.

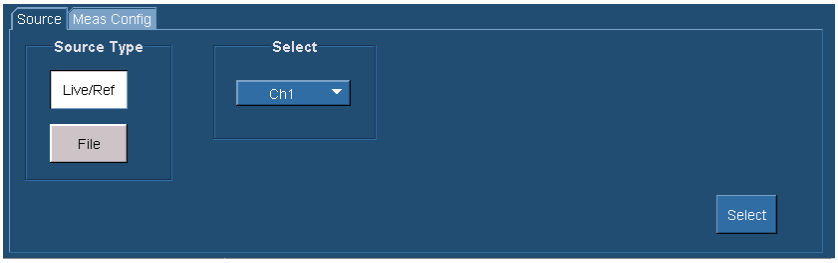


Figure 14: Configure Source menu

Source selections are dependent on the selected probe type. The selections are as follows:

If Differential is selected as Probe Type:

- **Live/Ref** source selection (uses single differential signal as data source)
  - Live channel selections–Ch1, Ch2, Ch3, Ch4
  - Reference waveform selections–Ref1, Ref2, Ref3, Ref4
- **File** source selection
  - File selection – Uses a single saved .csv as file as differential data source

If Single-Ended is selected as Probe Type:

- **Live/Ref** source selection (uses two single-ended signals as data source)
  - Live channel selections–(Ch1-Ch3), (Ch1-Ch4), (Ch2-Ch3), (Ch2-Ch4)
  - Reference waveform selections –Refx-Refy, where x and y are integers 1-4
- **File** source selection
  - File selection–Uses two saved .csv files as single-ended data source

3.5.6 Configure Clock Recovery

Use the **Measurements > Configure > Meas Config** menu to select the type of clock recovery to be used.

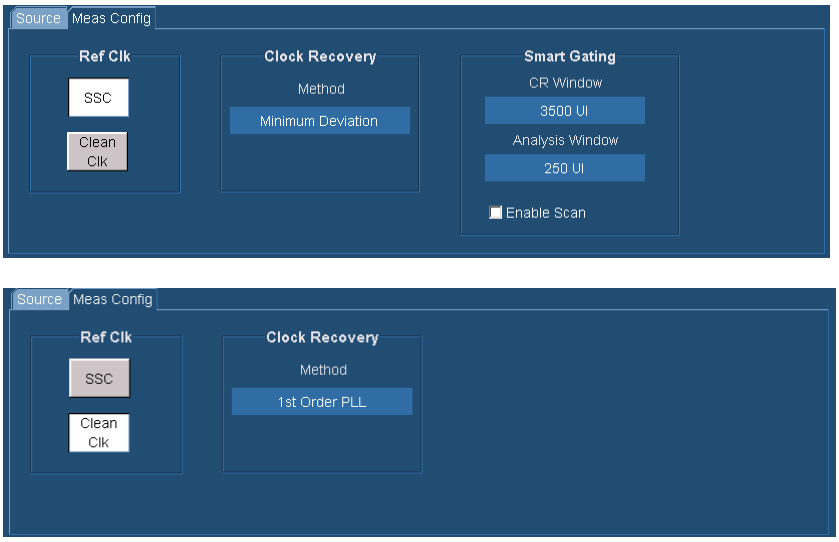


Figure 15: Measurement Configuration menu

Selections in the General Config panel depend on the specification that has been chosen. The selections are defined as follows:

If **Rev1.0a – 2.5 Gb/s** is selected as Standard:

- SSC (Scan Off) – 3500:250 clock recovery with no waveform scanning is used.
- SSC (Scan On) – 3500:250 clock recovery with waveform scanning is used.

If **Rev1.1 – 2.5 Gb/s** is selected as Standard:

- SSC (Scan Off) – 3500:250 clock recovery with no waveform scanning is used.
- SSC (Scan On) – 3500:250 clock recovery with waveform scanning is used.
- Clean Clock – A 1st Order SW PLL with a corner frequency of 1 MHz is used to recover the clock.

If **Gen2 – 5 Gb/s** is selected as Standard:

- SSC (Scan Off) – 3500:250 clock recovery with no waveform scanning is used.
- SSC (Scan On) – 3500:250 clock recovery with waveform scanning is used.
- Clean Clock – A 2nd Order SW PLL with a corner frequency of 1.5 MHz is used to recover the clock.

When to use SSC selection:

SSC is the only selection in Rev1.0a and is optional in the Rev1.1 and Gen2. It is to be used when a clean clock source is not available or if SSC is turned on in a system. The following describes how the clock is recovered using this technique:

- The "SmartGating" feature of the RT-Eye application is used to set up a software clock recovery window and an analysis window. This feature is available (and configurable) outside the PCI Express Compliance Module in the Measurements> Configure> SmartGating menu of the Serial Analysis module.
- The clock recovery window is 3500 consecutive UIs and the Mean of the UIs is used as the reference clock. The first 3500 UIs in the acquisition are used.
- An analysis window is established to be 250 UIs centered in the 3500 UI clock recovery window. The placement of mask is based on the median of the 250 UI analysis windows.
- Optionally, the "Scan On" check box can be selected. When checked, the clock recovery and analysis waveform will scan the waveform by stepping the 3500:250 window across the waveform in 100 UI steps. This technique is same as the PCI-SIG SigTest software, used to determine compliance over a singleshot waveform.

When to use the Clean Clock selection:

- The clean clock selection is not available when Rev1.0a specification is selected. It is optional when Rev1.1 or Gen2 Specification is selected. It should be used when a clean reference clock is available. This is usually in the case while testing PHY components and Add-In cards. As defined in the base specification, if a clean clock is available, the clock recovery function to be used is a TIE filter function (Figure 16). For Rev1.1 this function is a 1st order (20dB/decade rolloff) with a corner frequency of
  1.5 MHz. For Rev2.0, this function is specified as a 'brick wall' function with a transition from –60 dB to 0 dB at 1.5 MHz. The RT-Eye PCI Express compliance module implements a first order SW PLL, which is specified. For Rev2.0, a 2nd order PLL with .707 damping factor is used to approximate a brick wall function. The SW PLL BW is dependent on the edge density of the signal under test for which the algorithm assumes an edge density of 50%. If the edge density of the DUT were 50%, the PLL BW frequency would be set to correspond to the frequencies in Figure 16. However, for compliance testing, the transmitter is required to transmit the PCI Express Compliance Pattern that has an edge density of 75%. Thus the loop BW of the SW PLL is set to [(0.5/0.75) x *specified frequency*]. This results in a PLL loop BW of 1 MHz. The loop BW of the SW PLL can be changed in the test point file. If the edge density of signal under test is different than 75%, the loop BW should be changed to be compliant with the specification. Refer to Section 9 for additional information on using Dynamic Test Points.

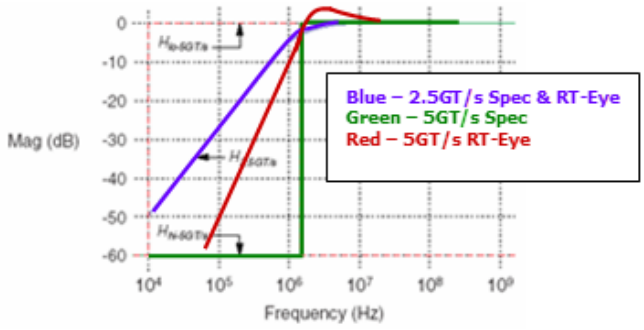


Figure 16: Clock recovery mask function in Rev2.0 base specification

3.5.7 Configure Plots

The plots in the PCI Express Module are configured automatically. If the **Jitter@BER** measurement is not selected, eye diagrams with masks will be displayed in the **Plot Summary** window (Figure 17a). The eye diagram can either be a double plot showing transition bit and non-transition bit or can be a single plot showing all bits depending on the test point selected.

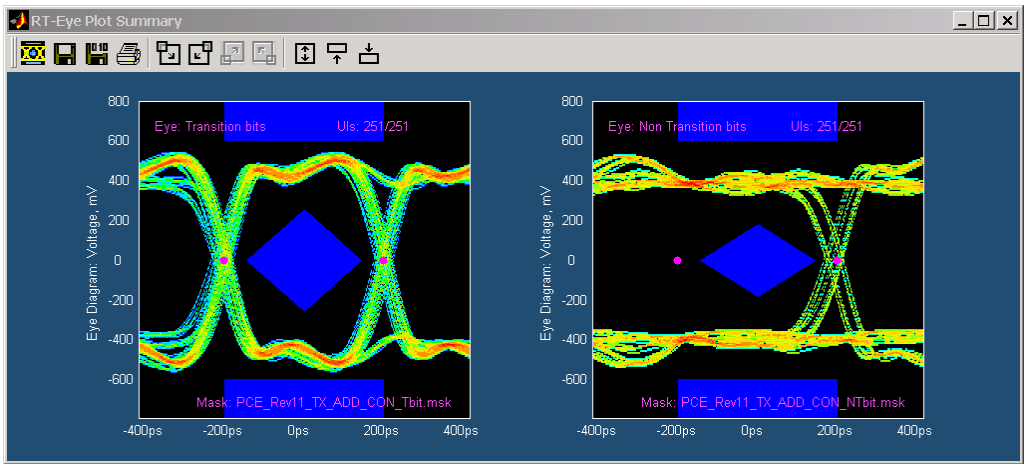


Figure 17a: Plot Summary when Jitter@BER measurement is not selected

If the **Jitter@BER** measurement is selected, then a Jitter Spectrum and Bathtub Curve are added to the **Plot Summary** window.

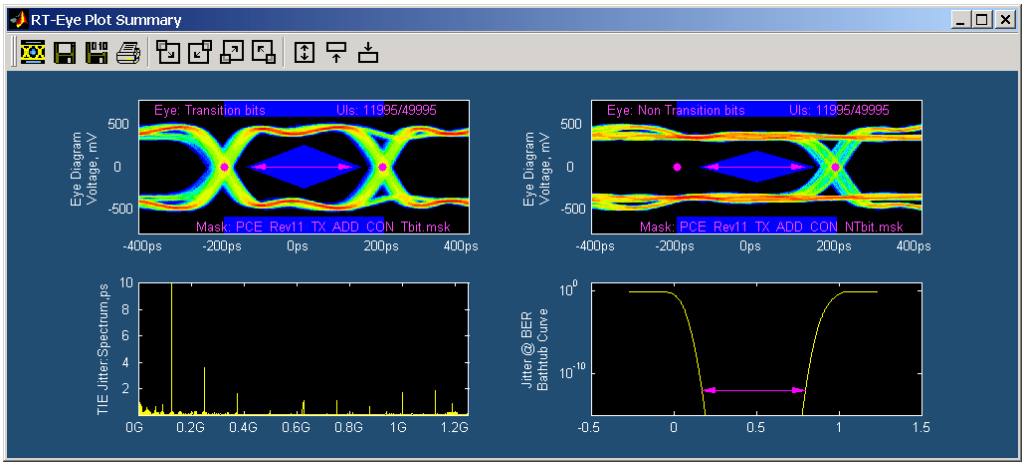


Figure 17b: Plot Summary when the Jitter@BER measurement is selected

4 PCI Express Transmitter Compliance Testing

This section provides the Methods of Implementation (MOIs) for Transmitter tests using a Tektronix real-time oscilloscope, probes, and the RT-Eye PCI Express compliance software.

4.1 Probing the link for TX compliance

Use probing configuration B from Section 3. Connect the positive leg of the differential signal to the '+' SMA connector and the negative leg of the differential signal to the '–' SMA connector on the P7300SMA series differential probing system.

Alternatively, use probe configuration A, to connect Ch1 and Ch3 to the inputs of an oscilloscope that has 20 GS/s sample rate available on two channels (TDS6604 or TDS6000B Series).

Since the link is broken and terminated into a 50 Ω load, the compliance pattern is defined in the base specification will be transmitted automatically.

4.2 TX Compliance Test Load

The compliance test load for driver compliance is shown in the base specification.

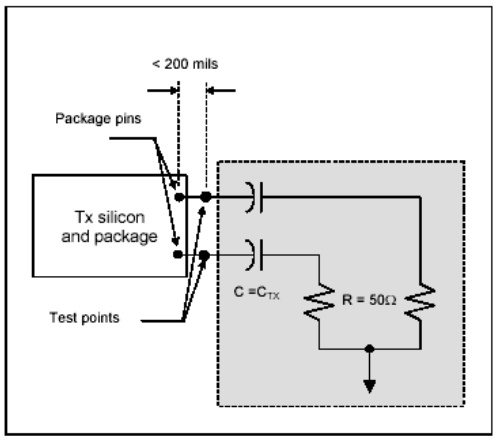


Figure 18: Driver compliance test load

4.3 Running a Transmitter (TX) Compliance Test

The MOI for each of the transmitter measurements is documented in the following sections. All transmitter compliance measurements can be selected and run simultaneously with the same acquisition. See Section 3 for more information on configuring the module to make measurements.

To perform a compliance test of all transmitter measurements:

1. Select the desired **Specification** from the Specification drop-down list.
2. Select the desired **Test Point** from the Test Point drop-down list.
3. In the Measurement Select menu (Figure 19), choose Single-Ended (for probe configuration A defined in Section 3) or Differential (for probe configurations B defined in Section 3) as the probe type.
4. Click **Configure** to configure the source and clock recovery method to be used.
5. Click **Source** tab to configure the data source.
6. Click **General Config** tab to select the desired clock recovery method.
7. Return the Measurement Select menu by clicking **Select**.

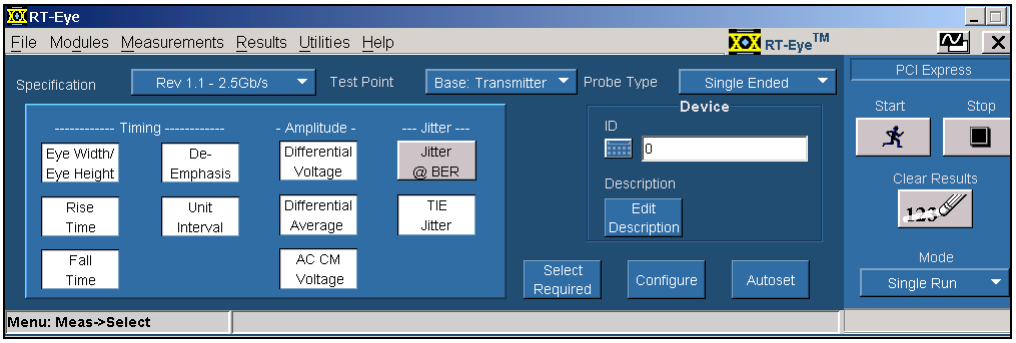


Figure 19: Measurements Select menu setup

8. Click **Select Required** and/or select desired measurements manually.
9. Click **Autoset** in the RT-Eye Measurement Select menu. This will automatically set up the oscilloscope vertical, horizontal, and measurement reference levels for the compliance test.
10. Click **Start**.

Figure 20 shows the result of a Transmitter Compliance test on a signal that passes the driver tests at all three TX compliance test points.

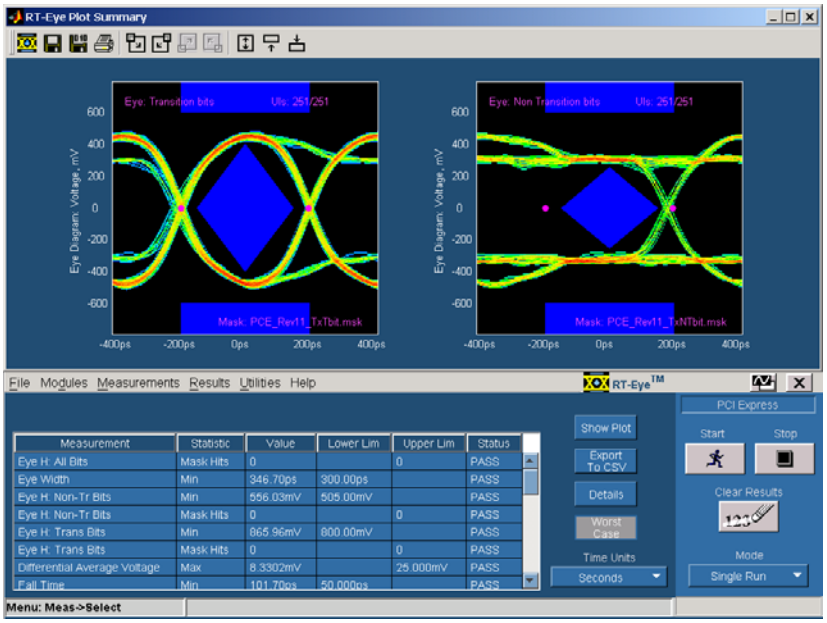


Figure 20: Result of a successful transmitter compliance test

4.3.1 TX Unit Interval Measurement MOI

Test Definition Notes from the Specification:

- UI (Unit Interval) is specified to be +/- 300 ppm

- UI does not account for SSC dictated variations

Definition: UI is defined in the base specification.

Limits:

Refer to Table 2 for specified limits on UI measurement.

Test Procedure:

Ensure that Unit Interval is selected in the Measurements > Select menu.

Measurement Algorithm:

This measurement is made over the Analysis Window of 250 consecutive bits (or over the entire record if the sw PLL is used) as defined in the Base Specification.

The Unit Interval measurement calculates the cycle duration of the recovered clock.

$$UI(n) = t_{R-CLK}(n+1) - t_{R-CLK}(n)$$

$$UI_{AVG} = Mean(UI(n))$$

Where:

t_{R-CLK} is a recovered clock edge

n is the index to UI in the waveform

4.3.2 TX Differential Pk-Pk Output Voltage MOI

Definition:

$V_{TX-DIFFp-p}$ (Differential Output Pk-Pk Voltage) is defined in the base specification. This measurement is solved by two measurements. One is Differential Peak Voltage measurement and the other is Eye Height: Transition Bits measurement. If you select Differential Voltage and Eye Width/Eye Height, you will get five measurements: Eye Height, Eye Height: Transition Bits, Eye Height: Non-Trans Bits, Eye Width and Differential Peak Voltage.

Test Definition Notes from the Specification:

- $V_{TX-DIFFp-p} = 2*|V_{TX-D+} - V_{TX-D-}|$

- Specified at the measurement point into a timing and voltage compliance test load as shown in the base specification and measured over specified number of UIs. Also refer to the transmitter compliance eye diagram shown in the base specification.

Limits:

Refer to Table 2 for specified limits on the $V_{TX-DIFFp-p}$ measurement.

Test Procedure:

Ensure that Differential Voltage and Eye Width/Eye Height are selected in the Measurements > Select menu.

Measurement Algorithm:

Differential Peak Voltage Measurement: The Differential Peak Voltage measurement returns two times the larger of the Min or Max statistic of the differential voltage waveform.

$$V_{DIFF-PK} = 2 * Max(Max(v_{DIFF}(i)); Min(v_{DIFF}(i)))$$

Where:

i is the index of all waveform values

v_{DIFF} is the differential voltage signal

Eye Height Measurement: The measured minimum vertical eye opening at the UI center as shown in the plot of the eye diagram. There are three types of eye height values:

Eye Height:

$$V_{EYE-HEIGHT} = V_{EYE-HI-MIN} - V_{EYE-LO-MAX}$$

Where:

$V_{EYE-HI-MIN}$ is the minimum of the high voltage at mid UI

$V_{EYE-LO-MAX}$ is the maximum of the low voltage at mid UI

Eye Height – Transition:

$$V_{EYE-HEIGHT-TRAN} = V_{EYE-HI-TRAN-MIN} - V_{EYE-LO-TRAN-MAX}$$

Where:

$V_{EYE-HI-TRAN-MIN}$ is the minimum of the high transition bit eye voltage at mid UI

$V_{EYE-LO-TRAN-MAX}$ is the maximum of the low transition bit eye voltage at mid UI

Eye Height – Non-Transition:

$$V_{EYE-HEIGHT-NTRAN} = V_{EYE-HI-NTRAN-MIN} - V_{EYE-LO-NTRAN-MAX}$$

Where:

$V_{EYE-HI-NTRAN-MIN}$ is the minimum of the high non-transition bit eye voltage at mid UI

$V_{EYE-LO-NTRAN-MAX}$ is the maximum of the low non-transition bit eye voltage at mid UI

4.3.3 TX De-Emphasized Differential Output Voltage (Ratio) MOI

Definition:

$V_{TX-DE-RATIO}$ (De-Emphasized Differential Output Voltage (Ratio)) is defined in the base specification.

Test Definition Notes from the Specification:

- This is the ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.

- Specified at the measurement point into a timing and voltage compliance test load as shown in the base specification over the specified number of UIs. Also refer to the transmitter compliance eye diagram shown the base specification.

Limits:

Refer to Table 2 for specified limits on the $V_{TX-DE-RATIO}$ measurement.

Test Procedure:

Ensure that **De-Emphasis** is selected in the **Measurements > Select** menu.

Measurement Algorithm:

The de-emphasis measurement calculates the ratio of any non-transition eye voltage (2nd, 3rd, etc. eye voltage succeeding an edge) to its nearest preceding transition eye voltage (1st eye voltage succeeding an edge). In Figure 21, it is the ratio of the black voltages over the blue voltages. The results are given in dB.

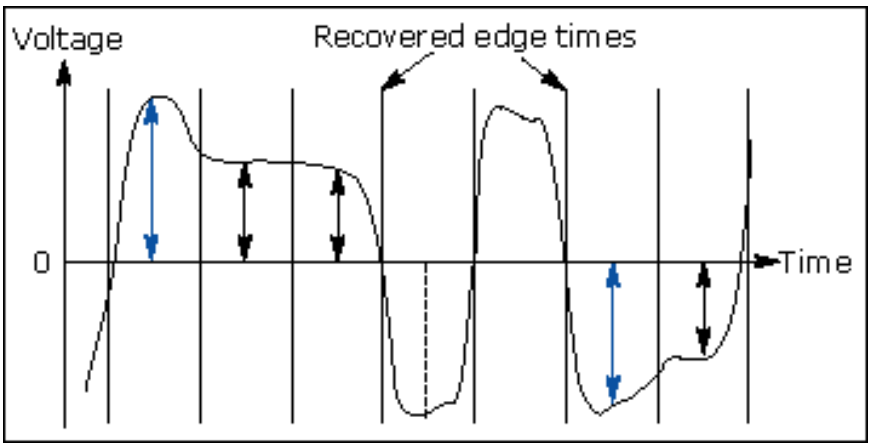


Figure 21: De-emphasis measurement

$$DEEM(m) = dB\left(\frac{v_{EYE-HI-NTRAN}(m)}{v_{EYE-HI-TRAN}(n)}\right)$$

or

$$DEEM(m) = dB\left(\frac{v_{EYE-LO-NTRAN}(m)}{v_{EYE-LO-TRAN}(n)}\right)$$

Where:

$v_{EYE-HI-TRAN}$ is the high voltage at mid UI following a positive transition

$v_{EYE-LO-TRAN}$ is the low voltage at mid UI following a negative transition

$v_{EYE-HI-NTRAN}$ is the high voltage at mid UI following a positive transition bit

$v_{EYE-LO-NTRAN}$ is the low voltage at mid UI following a negative transition bit

m is the index for all non-transition UIs

n is the index for the nearest transition UI preceding the UI specified by *m*

4.3.4 Minimum TX Eye Width MOI

Definition:

T_{TX-EYE} (Minimum TX Eye Width) is defined in the base specification. Note that the definition of the parameter Eye width changes from Rev1.x to the Rev2.0. See Section 4.3.9 for the Rev2.0 definition. For Gen1, the Eye width is a waveform histogram-based measurement that is defined as follows. For Rev2.0 T_{TX-EYE} is defined to be the Jitter Eye Opening which is described later.

Test Definition Notes from the Specification:

- The maximum Transmitter jitter can be derived as $T_{TXMAX-JITTER} = 1 - T_{TX-EYE}$.

- Specified at the measurement point into a timing and voltage compliance test load as shown in the base specification and measured over the specified number of UIs. Also refer to the transmitter compliance eye diagram shown in the base specification.

Note: The median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

Limits:

Refer to Table 2 for specified limits on the T_{TX-EYE} measurement.

Test Procedure:

Ensure that **Eye Width** is selected in the **Measurements > Select** menu.

Measurement Algorithm:

The *measured* minimum horizontal eye opening at the zero reference level as shown in the eye diagram.

$$T_{EYE-WIDTH} = UI_{AVG} - TIE_{Pk-Pk}$$

Where:

UI_{AVG} is the average *UI*

TIE_{Pk-Pk} is the Peak-Peak *TIE*

4.3.5 TX Median-to-Max Jitter MOI

Definition:

$T_{TX-EYEMEDIAN-to-MAXJITTER}$ (maximum time between the jitter median and maximum deviation from the median.) is defined in Rev1.0a of the base specification.

Limits:

Refer to Table 2 for $T_{TX-EYEMEDIAN-to-MAXJITTER}$ measurement.

Test Procedure:

Ensure that **TIE** is selected in the **Measurements > Select** menu.

Measurement Algorithm:

The measured time difference between a data edge and a recovered clock edge.

$$tie(n) = t_{R-DAT}(n) - t_{DAT}(n)$$

Where:

t_{DAT} is the original data edge

t_{R-DAT} is the recovered data edge (for example, the recovered clock edge corresponding to the UI boundary of t_{DAT})

n is the index of all edges in the waveform

4.3.6 TX Output Rise/Fall Time MOI

Definition:

$T_{TX-RISE}$, $T_{TX-FALL}$ (D+/D- TX Output Rise/Fall Time) is defined in the base specification.

Test Definition Notes from the Specification:

- Specified at the measurement point into a timing and voltage compliance test load as shown in the base specification and measured over the specified number of TX UIs.

- Measured between 20-80% at transmitter package pins into a test load for both V_{TX-D+} and V_{TX-D-}.

Limits:

Refer to Table 2 for specified limits on $T_{TX-RISE}$, $T_{TX-FALL}$ measurements.

Test Procedure:

Ensure that Rise Time and Fall Time are selected in the **Measurements > Select** menu.

Note: Rise/Fall time D+ and D- measurements show up when the probe type is single-ended. Rise Time measurements show up when differential probe type is used. Error in Rise/Fall time measurements includes bandwidth limitations of the system in some cases.

Measurement Algorithm:

Rise/Fall time measurement supported in the RT-Eye PCI Express Compliance Module is currently limited to only rising or falling edges of consecutive transitions (T_{F2} and T_{R2} in Figure 22) for transmitter measurements as defined in the Gen1 specification. The Gen2 specification introduces T_{F1} and T_{F2} in Figure 22. Rise/Fall Time is taken independently on each single-ended waveform sources when you use two single-ended probes as the signal source. Differential signal Rise/Fall Time show up when you select Differential probe type.

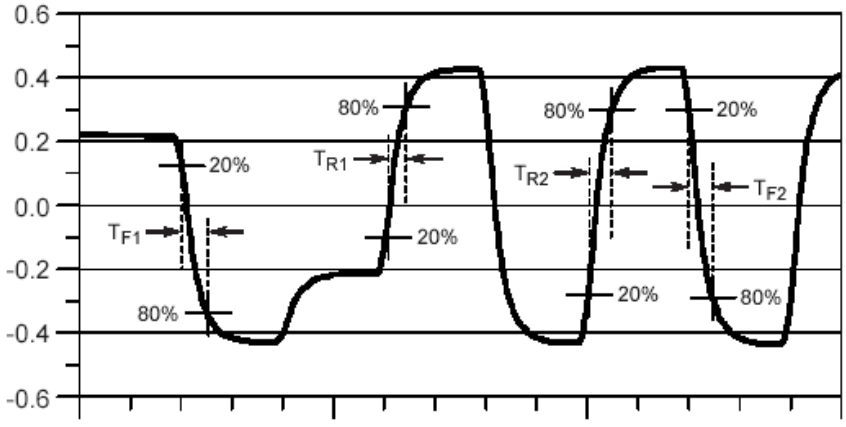


Figure 22: Rise/Fall Time measurement Gen2 specification. Only TR2 and TF2 are supported

Rise Time: The Rise Time measurement is the time difference between when the V_{REF-HI} reference level is crossed and the V_{REF-LO} reference level is crossed on the rising edge of the waveform.

$$t_{RISE}(n) = t_{HI+}(i) - t_{LO+}(j)$$

Where:

t_{RISE} is a Rise Time measurement

t_{HI+} is a set of t_{HI} for rising edges only

t_{LO+} is a set of t_{LO} for rising edges only

i and *j* are indexes for nearest adjacent pairs of t_{LO+} and t_{HI+}

n is the index of rising edges in the waveform

Rise Time for $v_{D+}(t)$ is as follows:

$$t_{D+RISE}(n) = t_{D+HI+}(i) - t_{D+LO+}(j)$$

and for $v_{D-}(t)$

$t_{D-FALL}(n) = t_{D-LO-}(i) - t_{D-HI-}(j)$

Fall Time: The Fall Time measurement is the time difference between when the V_{REF-HI} reference level is crossed and the V_{REF-LO} reference level is crossed on the falling edge of the waveform.

$$t_{FALL}(n) = t_{LO-}(i) - t_{HI-}(j)$$

Where:

t_{FALL} is a Fall Time measurement

t_{HI-} is set of t_{HI} for falling edge only

t_{LO-} is set of t_{LO} for falling edge only

i and *j* are indexes for nearest adjacent pairs of t_{LO-} and t_{HI-}

n is the index to falling edges in the waveform

Fall Time for $v_{D+}(t)$ is as follows:

$$t_{D+FALL}(n) = t_{D+LO-}(i) - t_{D+HI-}(j)$$

and for $v_{D-}(t)$, $t_{D-FALL}(n) = t_{D-LO-}(i) - t_{D-HI-}(j)$

4.3.7 TX AC Common Mode Output Voltage MOI

Definition:

$V_{TX-CM-ACp}$ (RMS AC Pk Common Mode Output Voltage) is defined in Rev1.0a Base Specification. The nomenclature ACp is retained to be consistent with the specification. However, the measurement is defined and reported by the PCI Express module as an RMS value, not a Pk value.

Test Definition Notes from the Specification:

$$V_{TX-CM-ACp} = RMS(|\frac{V_{TX-D+} + V_{TX-D-}}{2}| - V_{TX-CM-DC}) V_{TX-CM-DC} = DC_{(avg)} of\ |\frac{V_{TX-D+} + V_{TX-D-}}{2}|$$

- Specified at the measurement point into a timing and voltage compliance test load as shown in the base specification and measured over the specified number of TX UIs.

Limits:

Refer to Table 2 for specified limits on $V_{TX-CM-ACp}$ measurement.

Test Procedure:

Ensure that **AC CM Voltage** is selected in the **Measurements > Select** menu.

Note: This measurement is available only when the probe type is single-ended.

Measurement Algorithm:

AC CM RMS Voltage: The AC Common Mode RMS Voltage measurement calculates the RMS statistic of the common mode voltage waveform with the DC value removed.

$$v_{AC-RMS-CM}(i) = RMS(v_{AC-M}(i))$$

Where:

i is the index of all waveform values

$v_{AC-RMS-CM}$ is the RMS of the AC common mode voltage signal

v_{AC-M} is the AC common mode voltage signal

4.3.8 TX Delta DC Common Mode Voltage MOI

Definition:

$V_{TX-CM-DC-LINE-DELTA}$ (Absolute Delta of DC Common Mode Voltage between D+ and D-) is defined in the base specification.

Test Definition Notes from the Specification:

$$|V_{TX-CM-DC-D+} - V_{TX-CM-DC-D-}| \leq 25mV$$
$$V_{TXCM-DC-D+} = DC_{(avg)} of\ |V_{TX-D+}|$$
$$V_{TX-CM-DC-D-} = DC_{(avg)} of\ |V_{TX-D-}|$$

- Specified at the measurement point into a timing and voltage compliance test load as shown in the base specification and measured over the specified number of UIs.

Limits:

Refer to Table 2 for specified limits on $V_{TX-CM-DC-LINE-DELTA}$ measurement.

Test Procedure:

Ensure that Differential Average is selected in the Measurements > Select menu.

Measurement Algorithm:

The **Differential Average** measurement returns the mean of the differential voltage waveform.

$$V_{DIFF-AVG} = Mean(v_{DIFF}(i))$$

Where:

i is the index of all waveform values

v_{DIFF} is the differential voltage signal

4.3.9 TX Total Jitter@BER MOI

Definition:

The jitter eye opening T_{TX-EYE} is re-defined Gen2 specification to statistical relevance to 10^{-12} BER. A detailed definition can be found in the Gen2 base specification.

Test Definition Notes from the Gen2:

- Does not include SSC or Refclk. Jitter Includes Rj at 10^{-12}.

- Transmitter jitter is measured by driving the transmitter under test with a low jitter "ideal" clock and connecting the DUT to a reference load.

- Transmitter jitter must be post-processed with a filtering function that represents the worst case CDR tracking BW.

Limits:

Refer to Table 2 for specified limits on the T_{TX-EYE} measurement.

Test Procedure:

Ensure that **Jitter@BER** is selected in the **Measurements > Select** menu.

Measurement Algorithm:

Total jitter in the PCI Express Compliance Module uses the Arbitrary Pattern Jitter Algorithm in RT-Eye to establish T_{TX-EYE}. To understand the complete algorithm, one must understand RT-Eye's spectrum approach to jitter measurements. The RT-Eye PCI Express Compliance Module uses Spectral Analysis to estimate the Total Jitter. The Arbitrary Pattern method is used such that a repeating pattern is not required to achieve a jitter measurement result.

4.3.10 Spectrum Analysis Based Rj/Dj Separation on Repeating Pattern

Dj components can be identified in a jitter spectrum under a set of conditions. PJ will appear as spectral impulses regardless of conditions. DDJ and DCD will appear as spectral impulses provided that the data signal is a repeating pattern. The frequencies of DDJ and DCD spectral impulses are at harmonics of the (Bit Rate/Pattern length). The remaining spectral energy is attributed to Rj. Dj components are spectrally separated from Rj.

The Dj measurement is the peak-to-peak value of the inverse Fourier transform of the deterministic jitter spectral components, Tj is the total jitter which is composed of Dj and Rj. The Tj measurement calculates the peak-to-peak value of the total jitter. Rj is assumed to be near-Gaussian. The Rj measurement is the calculated RMS value of random jitter.

A Jitter PDF is formed by convolving a Gaussian distribution of Rj and Histograms of Dj. A Bathtub curve is calculated from the left and right side CDFs of the Jitter PDF. The Bathtub curve will yield TJ and Eye Opening ($T_{EYE-OPEN}$).

The application calculates the measurements using the following equations:

$$Dj = Max(Dj^{Time}) - Min(Dj^{Time})$$

$$Rj = RMS\left(tie - Dj^{Time}\right)$$

$$TJ_{PDF} = normalizedHistogram(Dj) * GaussianPDF(Rj)$$

$$TJ = TJ_{Max} - TJ_{MIN}$$

$$T_{EYE-OPEN} = UI - TJ$$

Where:

Dj is the deterministic jitter

Rj is the random jitter

TJ is the total jitter

TJ_{PDF} is the PDF of the total jitter

TJ_{MIN} is the minimum value at the bathtub curve at a given BER

TJ_{Max} is the maximum value at the bathtub curve at a given BER

Dj^{Time} is the is the time domain record of the Dj component of jitter obtained by performing an inverse FFT of the Dj components of the TIE spectrum

tie is the time domain record of measured TIE jitter

Additionally, Dj is further decomposed as follows:

$$PJ = Max(PJ^{Time}) - Min(PJ^{Time})$$

$$DCD = \left|Mean(DCDDDJ_{Rise}^{Time}) - Mean(DCDDDJ_{Fall}^{Time})\right|$$

$$DDJ = Max(DCDDDJ^{Time}) - Min(DCDDDJ^{Time}) - DCD$$

Where:

PJ is the periodic jitter

DCD is the duty cycle jitter

DDJ is the data dependent (or ISI) jitter

PJ^{Time} is the time domain record of the PJ component of jitter obtained by performing an inverse FFT of the PJ components of the TIE spectrum

$DCDDDJ^{Time}$ is the time domain record of the $DCD + DDJ$ component of jitter obtained by performing an inverse FFT of the $DCD + DDJ$ components of the TIE spectrum

$DCDDDJ^{Time}_{Rise}$ is $DCDDDJ^{Time}$ on rising edges only

$DCDDDJ^{Time}_{Fall}$ is $DCDDDJ^{Time}$ on falling edges only

4.3.11 Arbitrary Pattern Analysis Based Rj/Dj Separation

When data pattern is non-repeating, PJ still has a spectrum of impulses, while DCD+DDJ no longer has a spectrum of impulses. Therefore, Dj no longer has a spectrum of impulses.

The DCD+DDJ value is obtained through the arbitrary data pattern analysis method that is based on the assumption that any given bit is affected by a finite number of preceding bits. By averaging all events where the current bit is preceded by a particular bit sequence, for example the current bit is preceded by the bit sequence 1001101, the DCD+DDJ with such a pattern is obtained since PJ and RJ are not correlated to a particular data sequence and thus are averaged out.

If each bit is assumed to be affected by N preceding bits, there are a total of 2^N possible data sequences. The sequence length N is set to 5 in the PCI Express module (user configurable in the Serial Analysis module) because PCI Express is 8b/10b encoded. To get statistically sound average values, a population limit of 50 is set in the PCI Express module (user configurable in the Serial Analysis module) that prevents using an average value without enough population. Only DCD+DDJ values obtained from data sequences with a population above the limit are used to calculate DCD+DDJ values.

After each edge is associated with a DCD+DDJ value, with known total jitter, the PJ+Rj value for each bit is then obtained by subtracting DCD+DDJ from TJ.

Separation of DDJ and DCD from DCD+DDJ is the same as that in the spectrum based Rj/Dj separation method.

PJ and Rj are then separated from PJ+Rj and use the spectrum analysis method. PJ has a spectrum of impulses, and Rj has a flat spectrum. All the edges whose DCD+DDJ can not be determined because of their associated data sequences have low populations and are treated as if there are no edges when performing PJ and Rj separation.

The histogram of Dj is a convolution of the histogram of DCD+DDJ and the histogram of PJ.

All other aspects of the arbitrary pattern analysis based Rj/Dj separation are the same as those of the spectrum analysis based Rj/Dj separation.

4.3.12 TX Deterministic MOI (Using Dual-Dirac Model)

Definition:

Deterministic jitter $t_{TX\text{-}DJ\text{-}DD}$ using the Dual-Dirac model is defined in the Gen2 Base Specification.

Limits:

Refer to Table 2 for specified limits on Common the $t_{TX\text{-}DJ\text{-}DD}$ measurement.

Test Procedure:

Ensure that **Jitter@BER** is selected in the **Measurements > Select** menu.

4.3.13 Rj/Dj Separation Based on Dual-Dirac Model

Dual Dirac model based Rj/Dj separation method fits the Bathtub curve to a theoretical model of Rj and Dj where Rj is assumed to have a Gaussian distribution, Dj is assumed to have a distribution of two Dirac impulses with the same height. Curve fitting at different BER levels in Bathtub curve yields the standard deviation value of Rj and peak-to-peak value of Dj. The Bathtub curve is obtained from the spectrum analysis based or the arbitrary pattern analysis based Rj/Dj separation methods. Rj and Dj based on the Dual-Dirac model can be denoted as RJ_g and DJ_{dd}.

After RJ_g and DJ_{dd} are obtained, Tj can be calculated using

$$TJ(BER) = 2Q(BER) \times RJ_g + DJ_{dd}$$

where Q is the function of BER that has a value of about 7 when $BER = 10^{-12}$. Eye opening is computed in the same way as it is computed in the spectrum analysis based Rj/Dj separation.

Dual Dirac model based Rj/Dj separation method is used in PCI-Express module and FB-DIMM module.

Usually, actual Dj does not have a pure Dual-Dirac distribution. So the value of RJ_g is often greater than the value of Rj obtained from the spectrum analysis based or the arbitrary pattern analysis based Rj/Dj separation. The value of DJ_{dd} is often less than that of its corresponding one.

4.3.14 TX Waveform Eye Diagram Mask Test MOI

Test Definition Notes from the Specification:

- The TX eye diagram is defined in the base specification is specified using the passive compliance/test measurement load in place of any real PCI Express interconnect + RX component.

- There are two eye diagrams that must be met for the transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams will differ in voltage depending on whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit will always be relative to the transition bit.

- The eye diagram must be valid for the specified number of UIs.

Limits:

Mask geometries for each specification are defined by the limits in Table 2.

Test Procedure:

Waveform masks are plotted with eye diagrams for the selected test point. Mask violations are highlighted and counted by the application.

5 PCI Express Receiver (RX) Compliance Testing

This section provides the Methods of Implementation (MOIs) for receiver tests using a Tektronix real-time oscilloscope, probes, and the RT-Eye compliance software solution.

5.1 Probing the Link for RX Compliance

Use probing configuration (D) to probe the link differentially at a point close to the pins of the receiver device. Alternatively, use probing configuration (C) using the Ch1 and Ch3 inputs of an oscilloscope that has 20 GS/s sample rate available on two channels (TDS6604 and TDS6000B/C Series only).

5.2 Running a Complete RX Compliance Test

The MOIs for each RX test are documented in the following sections. All RX measurements can be selected and run simultaneously with the same acquisition. To perform a compliance test of all receiver measurements:

1. Select desired **Specification** from the Specification drop-down list.
2. Select desired **Test Point** from the Test Point drop-down list.
3. In the Measurement Select menu (Figure 23), choose Single-Ended (for probe configuration C defined in Section 3) or Differential (for probe configurations D defined in Section 3) as the **Probe Type**.
4. Click **Configure** to configure the source and clock recovery method to be used.
5. Click the **Source** tab to configure the data source.
6. Click the **General Config** tab to select the desired clock recovery method.
7. Return the Measurement Select menu by clicking **Select.**

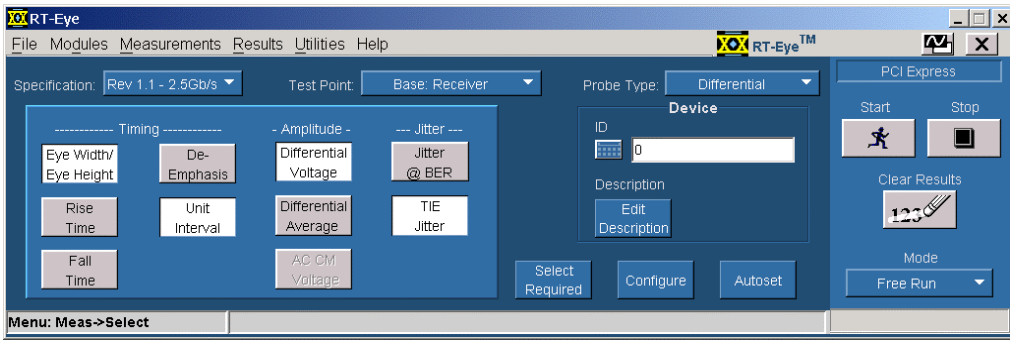


Figure 23: Measurements Select menu setup

8. Click **Select Required** and/or select the desired measurements manually.
9. Click **Autose**t in the RT-Eye Measurement Select menu. This will automatically set up the oscilloscope vertical, horizontal, and measurement reference levels for the compliance test.
10. Click **Start**.

Figure 24 shows the result of a transmitter compliance test on a signal that passes the driver tests at all three RX compliance test points.

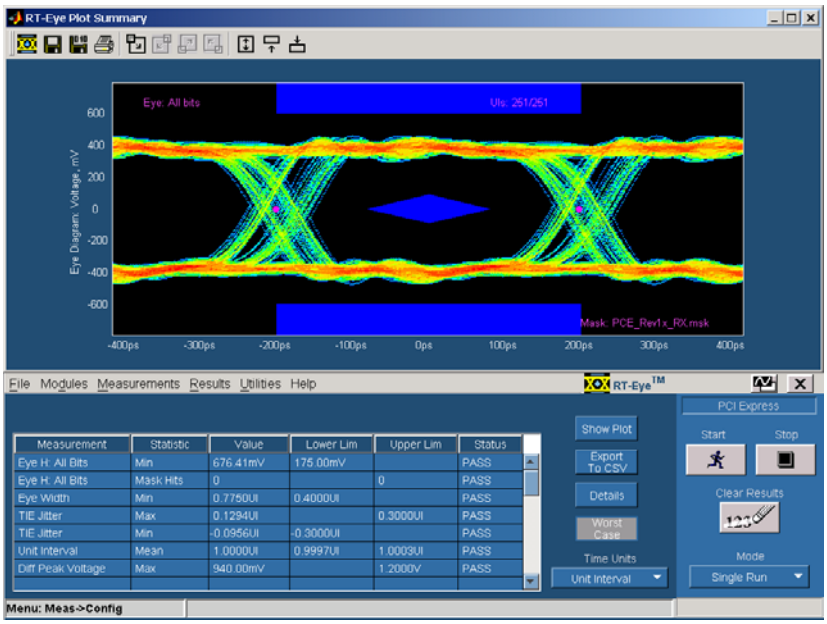


Figure 24: Result of a successful Compliance Test at the Receiver Pins

5.2.1 RX Unit Interval Measurement MOI

Refer to Unit Interval measurement in Section 4 of this MOI document. The MOI for the measurement of UI at the receiver is identical to measuring it at the transmitter, with the exception of the test point.

5.2.2 RX Differential Pk-Pk Input Voltage MOI

Definition:

$V_{RX-DIFFp-p}$ (Differential Input Pk-Pk Voltage) is defined in the base specification. This measurement is solved by two measurements: Differential Peak Voltage and Eye Height measurement.

Test Definition Notes from the Specification:

$V_{RX-DIFFp-p} = 2*|V_{RX-D+} - V_{RX-D-}|$

- Specified at the measurement point and measured over the specified number of UIs. The test load (defined in the base specification) should be used as the RX device when taking measurements. Also refer to the Receiver compliance eye diagram shown in the base specification. If the clocks to the RX and TX are not derived from the same reference clock, then the TX UI recovered from 3500 consecutive UIs must be used as a reference for the eye diagram.

Limits:

Refer to Table 3 for specified limits applicable to the $V_{RX-DIFFp-p}$ measurement.

Test Procedure:

Ensure that Differential Voltage and Eye Height/Eye Width are selected in the Measurements > Select menu.

Measurement Algorithm:

Refer to Section 4 of this MOI document for differential voltage measurement and eye height measurement algorithms.

Note: For receiver testing, eye height is measured on all UIs. There are no Eye Height: Transition Bits measurement and Eye Height: Non-Trans Bits measurement.

5.2.3 Minimum RX Eye Width MOI

Definition:

T_{RX-EYE} (Minimum RX Eye Width) is defined in the base specification.

Test Definition Notes from the Base Specification:

- The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = .6UI$.

- Specified at the measurement point and measured over the specified number of UIs. The test load in the base specification should be used as the RX device when taking measurements. Also refer to the Receiver compliance eye diagram shown in the base specification.

- A $T_{RX-EYE} = .40UI$ provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected over the specified number of UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total .6 UI jitter budget collected over the specified number of TX UIs.

Note: The median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

Limits:

Refer to Table 3 for specified limits applicable to the T_{RX-EYE} measurement.

Test Procedure:

Ensure that Eye Height/Eye Width is selected in the Measurements > Select menu.

Measurement Algorithm:

Refer to Section 4 of this MOI document for Eye Width measurement algorithm.

5.2.4 RX Median-to-Max Jitter MOI

Definition:

$T_{RX-EYEMEDIAN-to-MAXJITTER}$ (Maximum time between the jitter median and maximum deviation from the median.) is defined in the Gen1 base specification.

Test Definition Notes from the Specification:- Jitter is defined as the measurement variation of the crossing points ($V_{RXDIFFp-p} = 0V$) in relation to a recovered RX UI:

- The test load in the base specification should be used as the RX device when taking measurements. Also refer to the receiver compliance eye diagram shown in the base specification.

- A $T_{RX-EYE} = .40UI$ provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected over the specified number of UIs.

- $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total .6 UI jitter budget collected over the specified number of UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

Limits:

Refer to Table 3 for specified limits applicable to the $T_{RX-EYEMEDIAN-to-MAXJITTER}$ measurement.

Test Procedure:

Ensure that TIE Jitter is selected in the Measurements > Select menu.

Measurement Algorithm:

Refer to Section 4 of this MOI document for RX Median-to-Max Jitter measurement algorithm.

5.2.5 RX Total Jitter@BER MOI

Definition:

The jitter eye opening T_{RX-EYE} is re-defined Gen2 Base Specification to statistical relevance to 10^{-12} BER. A detailed definition can be found the Gen2 base specification.

Test Definition Notes from the Gen2:

- Minimum eye time at RX pins to yield a 10^{-12} BER.

- Receiver eye margins are defined into a 2x50 Ω reference load. A receiver is characterized by driving it with a signal whose eye opening is TRX_EYE, which is equivalent to generating a signal with a Tj of (1.0 UI – T_{RX_EYE}). The receiver under test then replaces the reference load, and the BER is observed.

- T_{RX-EYE} and $T_{RX-DJ-DD}$ are defined as tolerance parameters. In other words, T_{RX-EYE} defines the minimum eye that the receiver is expected to decode correctly. Another way of viewing T_{RX-EYE} is to consider that the amount of Tj that can be present is 1.0 UI - T_{RX-EYE} = 120 ps. $T_{RX-DJ-DD}$ defines the maximum amount of Dj that may be present in the Tj number of 120 ps implied by V_{RX-EYE}.

Note: T_{RX-EYE} defines an eye opening, while $T_{RX-DJ-DD}$ defines an eye closure.

Limits:

Refer to Table 3 for specified limits on the T_{RX-EYE} measurement.

Test Procedure:

Ensure that Jitter@BER is selected in the Measurements > Select menu.

Measurement Algorithm:

Refer to Section 4 for the Jitter@BER algorithm.

5.2.6 RX Deterministic Jitter@BER using Dual-Dirac model

Definition:

The jitter eye opening $T_{RX\_DJ\_DD}$ is redefined in Gen2 Base Specification to statistical relevance to 10^{-12} BER A detailed definition can be found in the Gen2 Base specification.

Test Definition Notes from the Gen2:

- Maximum Dj applied to receiver test circuit.

Limits:

Refer to Table 3 for specified limits on the $T_{RX\_DJ\_DD}$ measurement.

Test Procedure:

Ensure that Jitter@BER is selected in the Measurements > Select menu.

Measurement Algorithm:

Refer to Section 4 of this MOI document for the algorithm.

5.2.7 RX Waveform Eye Diagram Mask Test MOI

Test Definition Notes from the Specification:

- The RX eye diagram in the base specification is specified using the passive compliance/test measurement load in place of any real PCI Express RX component.

Note: In general, the minimum receiver eye diagram measured with the compliance/test measurement load will be larger than the minimum Receiver eye diagram measured over a range of systems at the input Receiver of any real PCI Express component. The degraded eye diagram at the input receiver is due to traces internal to the package as well as silicon parasitic characteristics, which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum receiver eye diagram expected at the input receiver-based on some adequate combination of system simulations and the return loss measured looking into the RX package and silicon.

- The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

Limits:

Mask geometries for each specification are defined by the limits in Table 3.

Test Procedure:

Waveform masks are plotted with eye diagrams for the selected test point. Mask violations are highlighted and counted by the application.

6 PCI Express Interconnect Test Point Testing

This section provides the Methods of Implementation (MOIs) for the test points outlined in Tables 4-9. These test points are defined at different interconnect points in the system between the transmitter and receiver. Interconnects supported are add-in card and system board test points for both desktop and ExpressModule, the cabling specification, and the ExpressCard specification. To perform a compliance test of all interconnect specific measurements:

1. Hook up the device to connector specific test fixture. For example Compliance Load Board (CLB) or Compliance Base Board (CBB).
2. Select the desired **Specification** from the Specification drop-down list.
3. Select the desired **Test Point** from the Test Point drop-down list.
4. In the Measurement Select menu (Figure 25), choose **Single-Ended** (for probe configuration A defined in Section 3) or **Differential** (for probe configurations B defined in Section 3) as the **Probe Type**.
5. Click **Configure** to configure the source and clock recovery method to be used.
6. Click the **Source** tab to configure the data source.
7. Click the **General Config** tab to select the desired clock recovery method.
8. Return the Measurement Select menu by clicking **Select**.

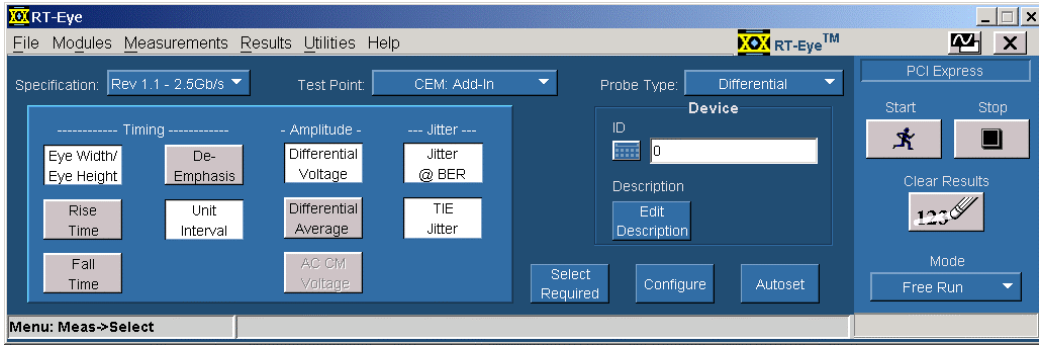


Figure 25: Measurements Select menu for add-in card test point

9. Click **Select Required** and/or select the desired measurements manually.
10. Click **Autoset** in the RT-Eye Measurement Select menu. This will automatically set up the oscilloscope vertical, horizontal, and measurement reference levels for the compliance test.
11. Click **Start**.

Figure 26 shows the result of a Transmitter Compliance test on a signal that passes the driver tests at all three RX compliance test points.

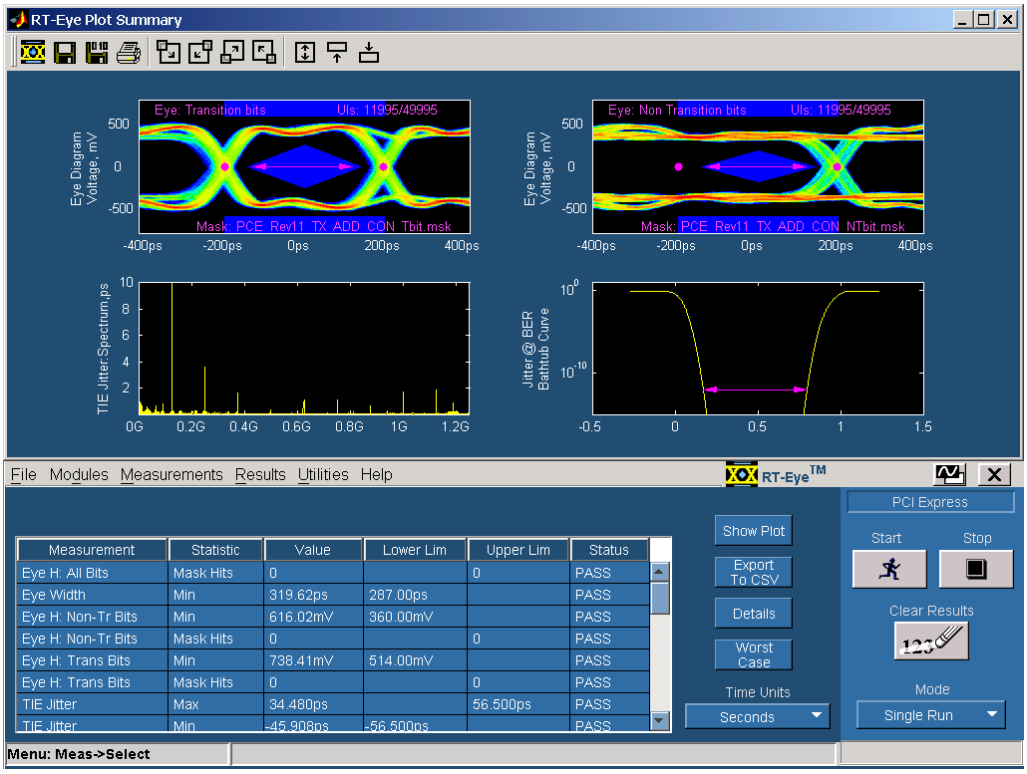


Figure 26: Successful add-in card compliance test

6.1 Unit Interval Measurement MOI

Refer to Section 4 of this MOI document. The MOI for the measurement of UI at the receiver is identical to measuring it at the transmitter, with the exception of the test point.

6.2 Transition and Non-Transition Bit Eye Height Measurement MOI

Definition:

V_{TxA}, V_{TxA_d}, V_{TxS}, and V_{TxS_d} are defined in the PCI Express CEM, Express Module, and cable specifications. V_{RxA} and V_{RxA_d} in the cabling specification also fall under the same definition, only they are defined at the receiver end of the cable.

Test Definition Notes from the Specification:

Rev1.0a CEM Specification:

- All links are assumed active while generating this eye diagram. Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level.

- The values are initially referenced to an ideal 100 Ω differential load at the end of the interconnect path on the edge-finger boundary of the add-in card (for add-in card measurement) or where the add-in card is mated with the connector (for system measurement). The eye diagram is defined and centered with respect to the jitter median. The jitter median should be calculated across any 250 consecutive UIs.

Rev1.1 CEM and Rev1.0 ExpressModule Specification:

-An ideal reference clock without jitter is assumed for this specification. All links are assumed active while generating this eye diagram.

- Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level.

- The values are referenced to an ideal differential load at the end of the interconnect path at the edge-finger boundary on the add-in card or the add-in card when mated to the connector. The eye diagram is defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are given in the PHY Electrical Test Considerations for PCI Express Architecture document.

Cabling Specification Rev0.4C:

- Rev1.1 CEM Notes plus:

- Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level.

- Transmitter path sdd21 is currently specified as 1.5 dB (1.25 GHz), which translates to a time domain equivalent of 1.67 dB (2.5 Gb/sec).

Limits:

Refer to Tables 4 to 11 for specified limits on V_{TxA}, V_{TxA_d}, V_{TxS}, and V_{TxS_d} for all interconnect and Table 9 for V_{RXA} and V_{RXA_d} measurements.

Test Procedure:

Ensure that Eye Height/Eye Width and Differential Voltage are selected in the Measurements > Select menu.

Measurement Algorithm:

Refer to Section 4 of this MOI document for measurement algorithms of eye height and differential voltage.

6.3 Eye Width Measurement MOI

Definition:

T_{TxA}, T_{TxS} for all interconnects that are defined in the PCI Express CEM, Express Module, and Cable Specifications. T_{RxA} in the cabling specification also falls under the same definition, only it is defined at the receiver end of the cable.

Test definition notes from the specification:

Rev1.0a CEM Specification:

-All links are assumed active while generating this eye diagram. Transition and non-transition bits must be distinguished in order to measure compliance against the deemphasized voltage level.

- The values are initially referenced to an ideal 100 Ω differential load at the end of the interconnect path on the edge-finger boundary of the add-in card [for add-in card measurement] or where the add-in card is mated with the connector [for system measurement]. The eye diagram is defined and centered with respect to the jitter median. The jitter median should be calculated across any 250 consecutive UIs.

Rev1.1 CEM and Rev 1.0 ExpressModule Specification:

- An ideal reference clock without jitter is assumed for this specification. All links are assumed active while generating this eye diagram.

- T_{TxA}, T_{TxS} is the minimum eye width. The sample size for this measurement is 106 UI. This value can be reduced to the (1UI -Jitter@BER) for simulation purposes at BER 10-12.

- The values are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the edge-finger boundary on the add-in card or the add-in card when mated to the connector. The eye diagram is defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are given in the PHY Electrical Test Considerations for PCI Express Architecture document.

Cabling Specification Rev0.4C:

- An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram.

- T_{TxA} and T_{RxA} is the eye width.

- The values are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the edge-finger boundary on the add-in card or the add-in card when mated to the connector. The eye diagram is defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are given in the PHY Electrical Test Considerations for PCI Express Architecture document.

Limits:

Refer to Tables 4 to 11 for specified limits on T_{TxA} and T_{TxS} for all interconnects and Table 9 for cable T_{RxA} measurements.

Test Procedure:

Ensure that Eye Width is selected in the Measurements > Select menu.

Measurement Algorithm:

Refer to Section 4 of this MOI document for measurement algorithms of Eye Width measurement.

6.4 Interconnect Median-to-Max Jitter and Total Jitter@BER MOI

Definition:

$J_{TX-MEDIAN-to-MAX-JITTER}$ is defined in Rev1.1 of the CEM specification. It is not explicitly defined in the Rev1.0a specification but can be derived by (1UI – Eye Width). Jitter@BER is introduced in Rev1.1 as discussed in the notes below.

Test definition notes from the specification:

Rev1.1 CEM Specification:

- $J_{TX-MEDIAN-to-MAX-JITTER}$ is the maximum median-to-max jitter outlier as defined in the PCI Express Base Specification, Revision 1.1. The sample size for this measurement is 106 UI. This value can be increased to (Jitter@BER) for simulation purpose at BER 10^{-12}.

Limits:

Refer to Table 4 for limits on $J_{TX-MEDIAN-to-MAX-JITTER}$ measurement.

Test Procedure:

-Ensure that **TIE** is selected in the Measurements > Select menu for $J_{TX-MEDIAN-to-MAX-JITTER}$.

-Ensure that **Jitter@BER** is selected in the Measurement > Select menu for 10^{-12} BER jitter estimation.

Measurement Algorithm:

Refer to Section 4 of this MOI document for jitter measurement algorithms.

7 PCI Express Reference Clock Compliance Measurements

This section provides the Methods of Implementation (MOIs) for reference clock tests. Reference Clock measurements for Rev1.1 are available in RT-Eye. For Rev2.0, refer to the tools library at www.pcisig.com.

7.1 Probing the Link for Reference Clock Compliance

Use probing configuration (B or D) to probe the link differentially at a point close to the pins of the reference clock. Alternatively, use probing configuration (A or C) using the Ch1 and Ch3 inputs of an oscilloscope can be used for reference clock measurements.

7.2 Running a Complete Reference Clock Compliance Test

The MOIs for each reference clock test is documented in the following sections. All reference clock measurements can be selected and run simultaneously with the same acquisition. To perform a compliance test of all receiver measurements:

1. Select **Measurements > Select**.
2. Select **Differential** (or Single-Ended) as the Probe Type, depending on your probe configuration.
3. Select **Reference clock** from the Test drop-down list.

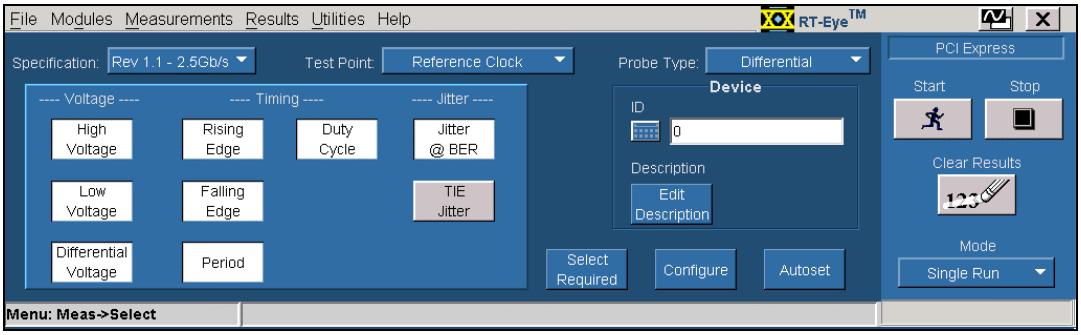


Figure 27: Measurements Select menu for reference clock test point

4. Select all or required measurements.
5. Click **Configure** to access the Configuration menus and set up signal source.
6. Click **Autoset** to set the horizontal scale, vertical scale, and reference levels for the reference clock measurements.
7. Click **Start**.

Figure 28 shows the result of a Reference clock Compliance test on a signal that passes the reference clock tests.

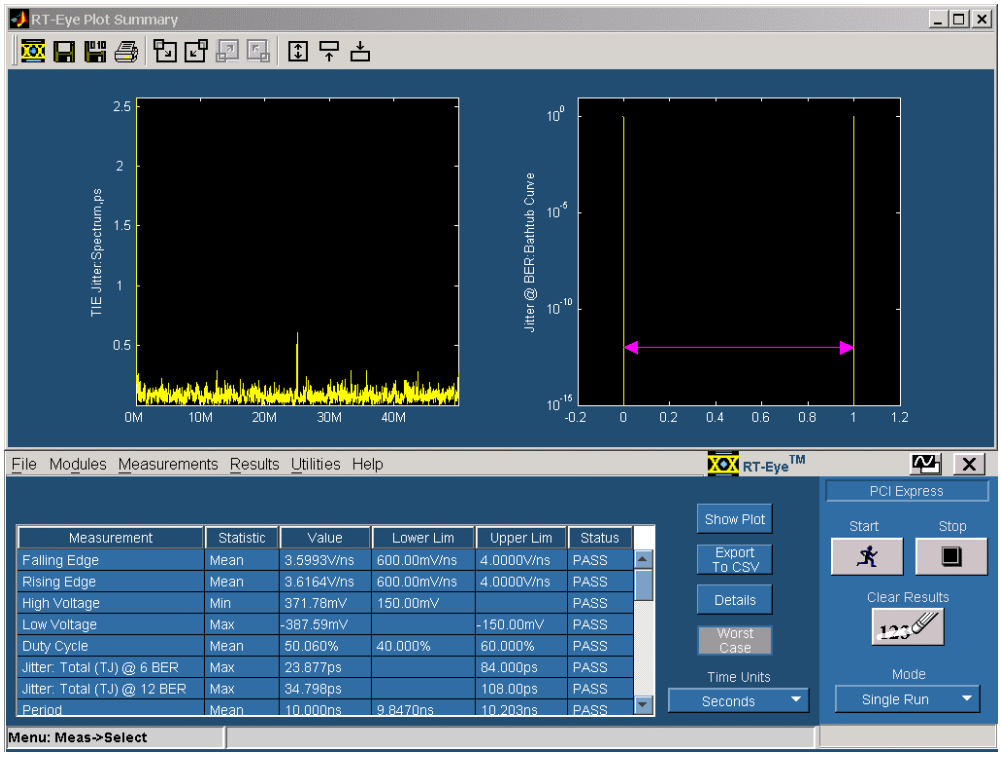


Figure 28: Result of a completed compliance test at the reference clock test point

7.2.1 Reference Clock Frequency Measurement Test MOI

Test Definition Notes from the Specification:

- Measurement is taken from differential waveform.

- Defines as the absolute minimum or maximum instantaneous period. This includes cycle to cycle jitter, relative PPM tolerance, and spread spectrum modulation.

Limits:

Refer to Table 12 for specified limits on absolute period measurement (T_{PERIOD_ABS}).

Test Procedure:

Ensure that **Period** is selected in the **Measurements > Select** menu**.**

Measurement Algorithm:

Measurement of period is defined in the specifications as follows:

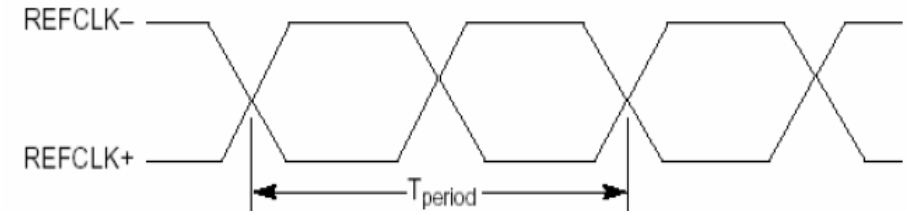


Figure 29: Reference clock period

7.2.2 Reference Clock Differential Voltage Hi and Lo Test MOI

Test Definition Notes from the Specification:

Measurement is taken from a differential waveform.

Limits:

Refer to Table 12 for specified limits on absolute period measurement (V_{IH}, V_{IL})

Test Procedure:

Ensure that High Voltage and Low Voltage are selected in the **Measurements** > **Select** menu.

Measurement Algorithm:

The High Amplitude measurement calculates the mode of all differential waveform values greater than zero.

$$V_{HI} = Mode(v_{DIFF}(i) > 0)$$

Where:

v_{DIFF} is differential voltage signal

i is the index of all waveform values

The Low Amplitude measurement calculates the mode of all differential waveform values greater than zero.

$$V_{LO} = Mode(v_{DIFF}(i) < 0)$$

Where:

v_{DIFF} is differential voltage signal

i is the index of all waveform values

7.2.3 Reference Clock Differential rise and fall edge rates test MOI

Test Definition Notes from the Specification:

-Measurement is taken from a differential waveform.

-Measured from -150 mV to +150 mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing.

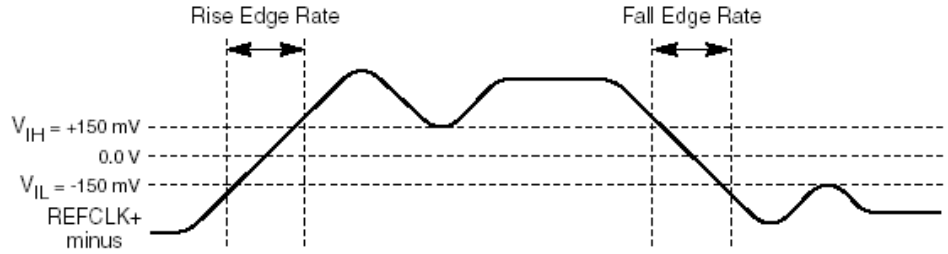


Figure 30: Ref Clock Rise/Fall time calculation

Limits:

Refer to Table 12 for specified limits on Absolute Period Measurement (*Rise Edge Rate, Fall Edge Rate)*

Test Procedure:

Ensure that Rising Edge and Falling Edge are selected in the **Measurements > Select** menu.

Measurement Algorithm:

The Rise and Fall Time are calculated over the 300 mV window, which is centered at differential 0 V. The rise/fall edge rate V/ns = 300 mV/rise/fall Time.

7.2.4 Reference clock Duty cycle Test MOI

Test Definition Notes from the Specification:

Measurement is taken from a differential waveform.

Limits:

Refer to Table 12 for specified limits on absolute period measurement (*Duty Cycle).*

Test Procedure:

Ensure that **Duty Cycle** is selected in the **Measurements > Select** menu.

Measurement Algorithm:

The Duty Cycle measurement calculates the ratio of the positive of the cycle relative to the period.

$$D_n^+ = W_n^+ / P_n^{Clock}$$

Where

Where*:* D^+ is the positive duty cycle

W^+ is the positive pulse width

P^{Clock} is the period

7.2.5 Reference Clock Jitter Test MOI

Test Definition Notes from the Specification:

Reference clock jitter is assumed to be entirely random in nature, so there is no need to define separate Dj or Tj terms.

Limits:

Refer to Table 10 for specified limits on random and Total Jitter Measurement values on reference clock (Jitter @ 10^{-12} BER, Jitter @ 10^{-6} BER, TCLK_RJ)

Test Procedure:

Ensure that **Jitter@BER** is selected in the **Measurements > Select** menu.

Measurement Algorithm:

The phase jitter of the reference clock is to be measured using the following clock recovery function

$$H(s) = \left[H_1(s) - H_2(s) * e^{-s*t\_delay}\right] \cdot H_3(s)$$

where:

$$H_1(s) = \frac{2s\zeta\omega_1 + \omega_1^2}{s^2 + 2s\zeta\omega_1 + \omega_1^2},$$

$$H_2(s) = \frac{2s\zeta\omega_2 + \omega_2^2}{s^2 + 2s\zeta\omega_2 + \omega_2^2},$$

$$H_3(s) = \frac{s}{s + \omega_3},$$

$$\zeta = 0.54$$

$$\omega_1 = \frac{2 * \pi * 22 \cdot 10^6}{\sqrt{1 + 2\zeta^2 + \sqrt{\left(1 + 2\zeta^2\right)^2 + 1}}} Rad / s$$

$$\omega_2 = \frac{2 * \pi * 1.5 \cdot 10^6}{\sqrt{1 + 2\zeta^2 + \sqrt{\left(1 + 2\zeta^2\right)^2 + 1}}} Rad / s$$

$$\omega_3 = 2 * \pi * 1.5 \cdot 10^6 \; Rad / s$$

$$t\_delay = 10 \cdot 10^{-9} \; s$$

8 Using SigTest

The SigTest import feature in the PCI Express module allows the user to take advantage of the Autoset features of RT-Eye and automate the process of performing a compliance test using the SigTest software offered by the PCI SIG. The SigTest Software is available at the PCI-SIG Web site at: http://www.pcisig.com/specifications/pciexpress/compliance/compliance_library

After downloading the SigTest software and installing it on your TDS oscilloscope, the SigTest software appears in C:\Program Files\SigTest or a similarly named directory.

To use SigTest, to perform the compliance test, follow these steps:

1. Select **Use SigTest** from the Specification drop-down list.
2. Select Differential or Single-Ended from the **Probe Type** drop-down list.
3. Go to the **Configure > SigTest Version** tab to import and name the SigTest version you would like to use. Note that you can import multiple versions of SigTest as they become available from the PCI SIG. The **Output Directory** field is where the SigTest results will be saved.

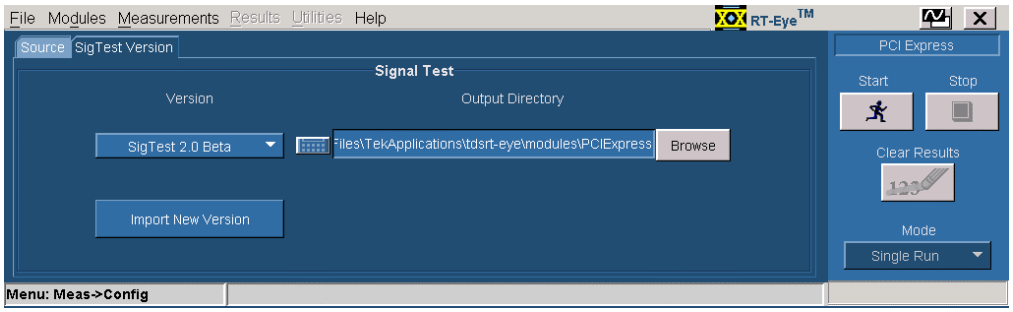


Figure 31: SigTest Version tab in the configure menu

4. To import and name a new SigTest version, click **Import New Version** using the browser to locate the version of SigTest to import.

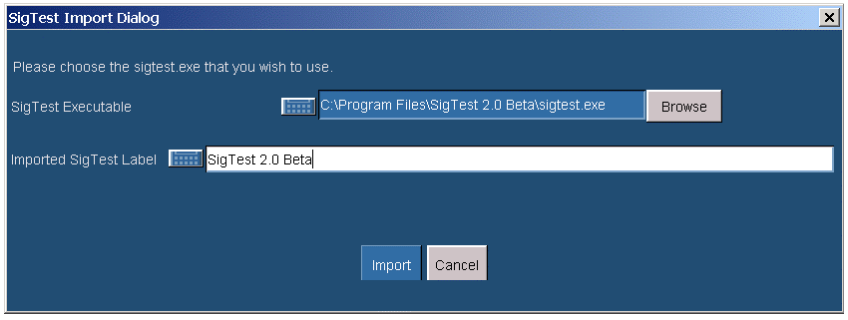


Figure 32: SigTest Import dialog box

5. Click **Browse** and select the SigTest Executable to be used.

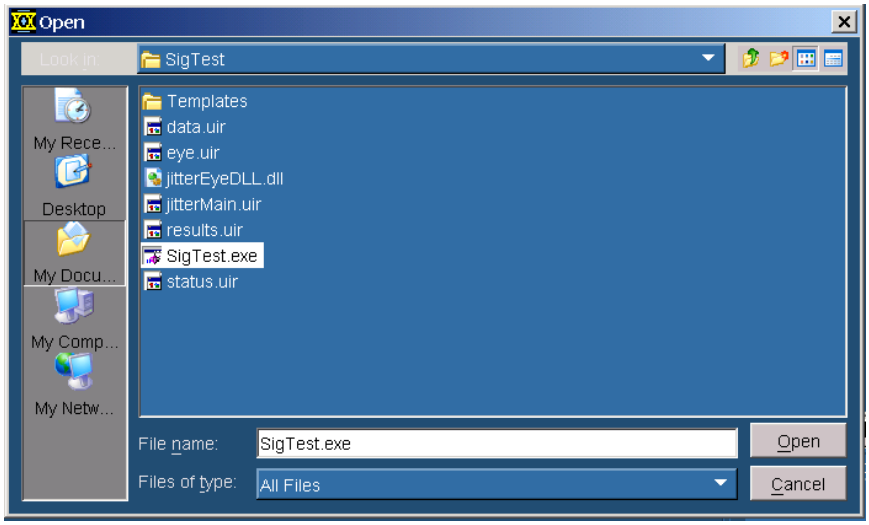


Figure 33: SigTest Import Dialog

6. Click the **Source** tab to select the data file input format. The source type is Live/Ref or File.

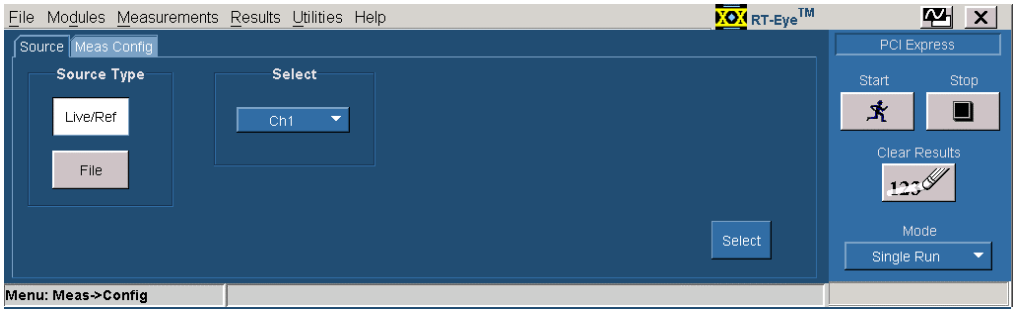


Figure 34: Configure > Source Tab

7. Click **Select** to return to the Measurement > Select menu.
8. Click **Autoset** to optimize vertical and horizontal oscilloscope settings for SigTest.

9. Click **Run** to launch SigTest and automatically import data waveforms into SigTest. Figure 35 shows the result after data is verified and run through SigTest.

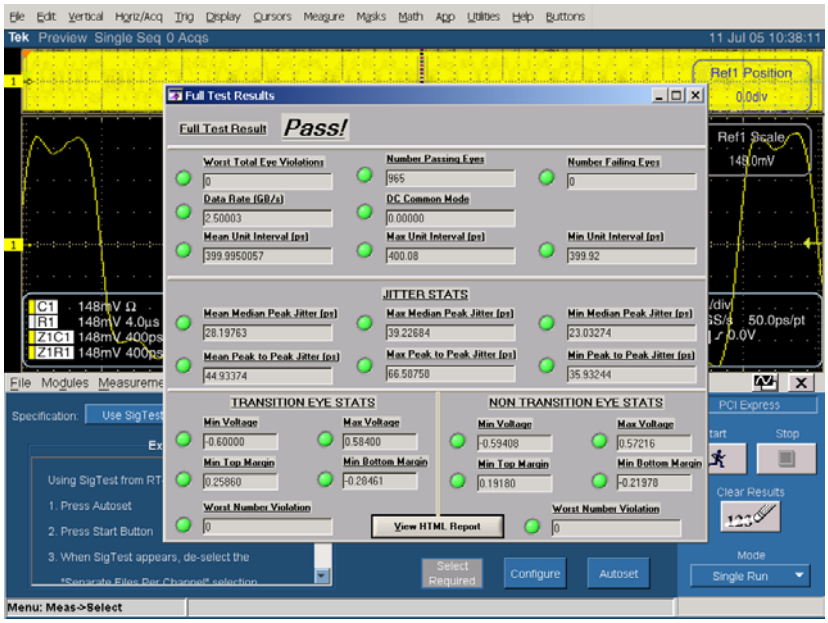


Figure 35: Result of running SigTest on live channel input

9 Using Dynamic Test Points

The Dynamic Test Point files used in the PCI Express module are designed to provide a means for advanced users to develop their own test points in the module. Usage of the dynamic test point will be demonstrated in the form of an example.

PCI Express Gen2 is at Rev0.3. But it is likely that masks and measurement limits may change before this specification reaches maturity. In PCI Express Gen2 Specification, it is required that measurements must de-convolve effects of compliance test board to yield an effective measurement at the TX pins. In the absence of de-convolving the test fixture from the measurement using some sort of equalization function, measurement masks and limits need to be de-rated to consider the effects of the loss characteristics in both the test fixture and the cables being used to make the measurement. In the following example, the transmitter test point in the Gen2 – 5 Gb/s (Base: Transmitter) will be modified to account for loss in the test system. The waveform masks and jitter limits will be de-rated and the test point file will be renamed Base_TX_2.0_Derated. Once the test point file is modified and saved in the proper folder, the new test point will show up in the Test Point menu drop-down in the PCI Express Compliance module. The following shows the format of the Gen2 TP file found at:

C:\Program Files\TekApplications\tdsRT-Eye\modules\PCIExpress\TestPoint

on the instrument where the module is installed.

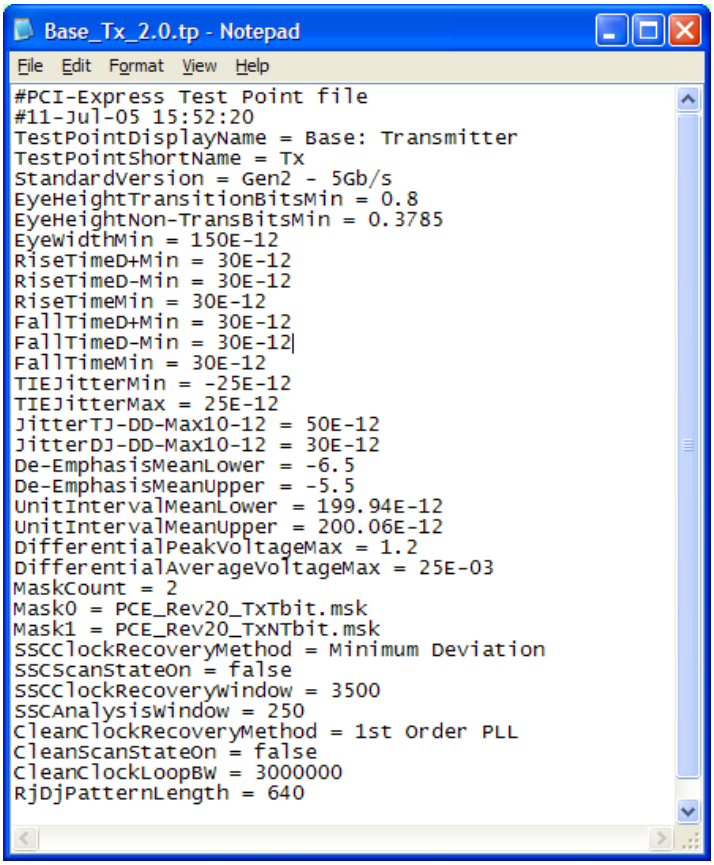


Figure 36 – Standard Gen2 TX test point file

9.1 Test Point File Syntax

The test point file can be broken down into the following syntax:

Header Information (comment lines) used to document description and date of test point file:

#PCI-Express Test Point file

#11-Jul-05 15:52:20

Test Point display name that shows up in the test point drop-down list:

TestPointDisplayName = Base: Transmitter

Standard Version that determines in which standard version list the test point will appear:

StandardVersion = Gen2 - 5 Gb/s

Test point short name that determines whether or not transition and non-transition bits will be separated. Choices are TX (Tbits and NTbits separated) and RX (Tbits and NTbits not separated):

TestPointShortName = TX

Measurement limits that determine pass/fail criteria and whether the measurement will show up as selected when Select Required is pressed:

EyeHeightTransitionBitsMin = 0.8

EyeHeightNon-TransBitsMin = 0.3785

EyeWidthMin = 150E-12

RiseTimeD+Min = 30E-12

RiseTimeD-Min = 30E-12

RiseTimeMin = 30E-12

FallTimeD+Min = 30E-12

FallTimeD-Min = 30E-12

FallTimeMin = 30E-12

TIEJitterMin = -25E-12

TIEJitterMax = 25E-12

JitterTJ-DD-Max10-12 = 50E-12

JitterDJ-DD-Max10-12 = 30E-12

De-EmphasisMeanLower = -6.5

De-EmphasisMeanUpper = -5.5

UnitIntervalMeanLower = 199.94E-12

UnitIntervalMeanUpper = 200.06E-12

DifferentialPeakVoltageMax = 1.2

DifferentialAverageVoltageMax = 25E-03

Number and location of Masks:

MaskCount = 2

Mask0 = PCE_Rev20_TxTbit.msk

Mask1 = PCE_Rev20_TxNTbit.msk

Note: PCI Express Mask files are located at:

C:\TekApplications\tdsrt-eye\Masks\PCI Express on the instrument that the module is installed. The following is the contents of PCE_Rev20_TxTbit.msk. Note that .msk file format is used by both RT-Eye and the instrument firmware in mask testing. The only parameters in the .msk file that RT-Eye uses are the highlighted mask vertices shown in bold font.

:MASK:USER:AMP 100.0000E-3;

:MASK:USER:PATTERNBITS 1;

:MASK:USER:PRESAMPBITS 0;

:MASK:USER:WID 400.0000E-12;

:MASK:USER:HSCA 62.5000E-12;

:MASK:USER:HTRIGPOS 500.0000E-3;

:MASK:USER:LAB "User Mask";

:MASK:USER

:TRIGTOSAMP 0.0000;

:MASK:USER:RECO 5000;

:MASK:USER:VSCA 200.0000E-3;

:MASK:USER:VPOS 0.0000;

:MASK:USER:VOFFS 0.0000;

:MASK:USER

:BITR 5.000E+9;

:MASK:USER

:SERIALTRIG NRZ;

:MASK:USER:SEG1:POINTS -100.0000E-12,600.0000E-3,100.0000E-12,600.0000E-3,100.0000E-12,800.0000E-3,-100.0000E-12,800.0000E-3;

:MASK:USER:SEG2:POINTS -75.0000E-12,0.0000,0.0000,-400.0000E-3,75.0000E 12,0.0000,0.0000,400.0000E-3;

:MASK:USER:SEG3:POINTS -100.0000E-12,-800.0000E-3,100.0000E-12, 800.0000E-3,100.0000E-12,-600.0000E-3,-100.0000E-12,-600.0000E-3;

:MASK:AUTOSET:STANDARD PCIEXPRESS_Xmit;

Clock recovery and windowing parameters when SSC is selected in the Measurement Configuration menu:

SSCClockRecoveryMethod = Minimum Deviation

SSCScanStateOn = false

SSCClockRecoveryWindow = 3500

SSCAnalysisWindow = 250

Clock recovery and pattern length used when Clean Clock is selected in the Measurement Configuration menu:

CleanClockRecoveryMethod = 1st Order PLL

CleanScanStateOn = false

CleanClockLoopBW = 6670000

RjDjPatternLength = 640

9.2 Creating the New Test Point

In this example, the Test Point and mask files will be copied and given new names. A text editor is used to modify their contents.

The new TP file (Figure 37) is saved to the folder:

C:\Program Files\TekApplications\tdsRT-Eye\modules\PCIExpress\TestPoint

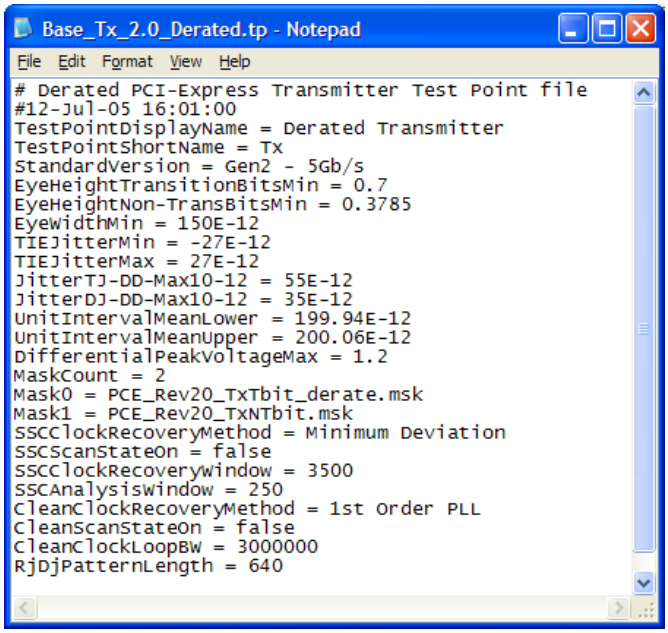


Figure 37: De-rated transmitter test point file – Base_TX_2.0_Derate.tp

The following changes are made to SEG2 of the Mask file:

:MASK:USER:SEG2:POINTS **-70.0000E-12**,0.0000,0.0000**,-350.0000E-3**,**70.0000E-12**,0.0000,0.0000,**350.0000E-3**;

This de-rates the horizontal mask limit from 150 ps to 140 ps and the vertical mask limit from 800 mV to 700 mV.

The new mask file is saved to the folder:

C:\TekApplications\tdsrt-eye\Masks\PCI Express as filename <PCE_Rev20_TxTbit_derate.msk>

9.3 Running a test with the new DTP

After the preceding file changes are made, when RT-Eye software is run, the new DTP is loaded into the PCI Express Compliance Module.

Figure 38: "De-rated Transmitter" DTP is now in the test point menu

To run the test, perform the following steps:

1. Go to the PCI Express Module
2. Select **Gen2 – 5 Gb/s** as the specification.
3. Select the new Test Point **De-rated Transmitter** from the Test Point drop-down list.
4. Click **Select Required** – Notice that measurements removed from the Test Point file are no longer selected.
5. Click **Start**. The results appear as shown in Figure 39. Notice that the new de-rated mask now appears as the Tbit mask and the upper and lower limits are the new values entered into the DTP file.

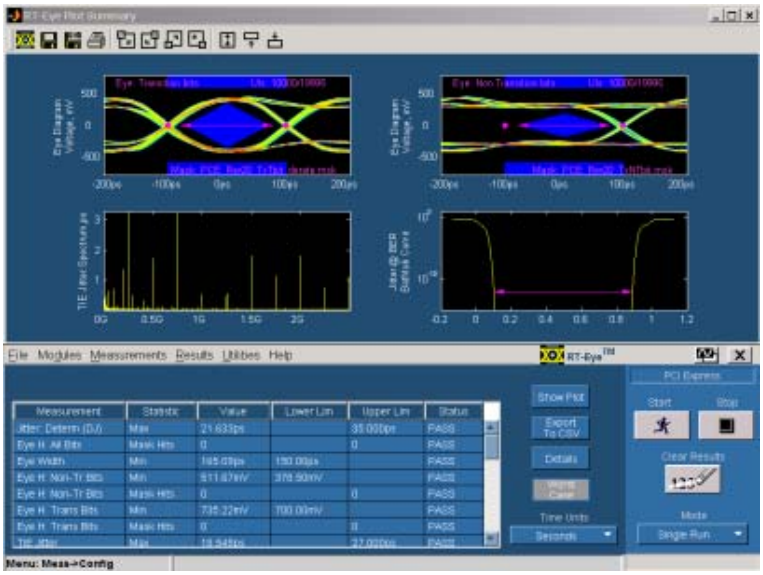


Figure 39: Result of de-rated transmitter test

10 Giving a Device an ID

The PCI Express Compliance module provides a graphical user interface (See Figure 38) for entering a device ID and description. Data entered here will appear on the compliance report and is recommended for device tracking.

11 Creating a Compliance Report

To create a compliance report, select **Utilities** > **Reports**. The Report Generator utility can create a complete report of the compliance test.

12 Further Analysis Techniques

Refer to the RT-Eye Quick Start Guide or Online Help for additional analysis techniques.

13 Ensuring Compliance over specified population

The Rev1.0a specification states that measurements are to pass the compliance statements over any 250 consecutive UIs. The Rev1.0a was ambiguous about the number of UIs needed to achieve compliance. The 3500:250 scan mode on a single acquisition has become the standard way of achieving compliance at industry plug fests. Rev1.1 of the specification has explicitly called out 10^6 as the population needed to achieve compliance. While the specification does not require 1Million consecutive unit intervals to be acquired, using a long enough record length to capture 1Million UIs will insure repeatable measurements and allow you save a single shot acquisition of the specification compliant acquisition for future analysis. In order to analyze 1Million unit intervals in RT-Eye, the 'Probe Type' must be set to Differential as described in section 3.5.3. This can be done using a differential probe on Ch1 (probe configurations B and D in Section 3.2) as the source. If the signal is probed single ended using Ch1 and Ch3 (as in probe configurations A and C in Section 3.2), then a Math waveform (Math1 = Ch1 – Ch3) can be used to perform the 1Million UI test.

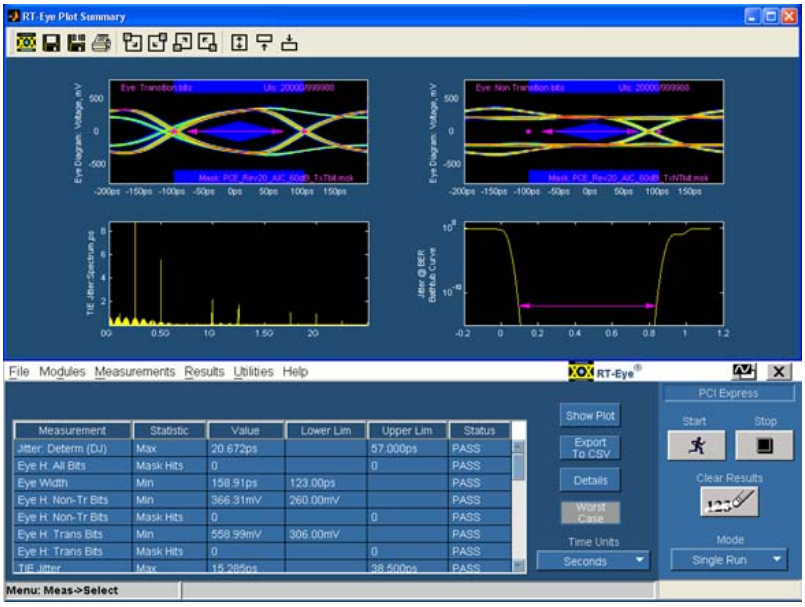


Figure 40: Result from a 1Million UI test on 5GT/s signal.